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TEST REPORT
AS/NZS 4777.2
Grid connection of energy systems via inverters

Report Reference No. ....:	220803032SHA-001
Tested by (name + signature) ....:	Billy Chen ………………………………
Approved by (name + signature) ......:	Sleif Sui ………………………………
Date of issue....................................:	2022-09-30
Contents …………………………...:	125 pages
Testing Laboratory ....:	Intertek Testing Services Shanghai
Address...:	Building No.86, 1198 Qinzhou Road (North), Shanghai 200233, China
Testing location / address.................:	Same as above
Applicant's name ....:	Afore New Energy Technology (Shanghai) Co., Ltd.
Address...:	Build No.7, 333 Wanfang Road, Minhang District, Shanghai. China. 201112
Test specification:	
Standard ....:	AS/NZS 4777.2: 2020+Amd 1:2021
Test procedure.................................:	Australia registration
Non-standard test method…………..:	N/A
Test Report Form/blank test report	
Test Report Form No. ....:	TTRF_AS_4777.2_V3.0
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Test item description ....:	Grid connected hybrid inverter
Trade Mark ....:	Afore
Manufacturer....................................:	Same as applicant
Model/Type reference.......................:	AF*-SL-1 (*= 1K, 1.5K, 2K, 2.5K, 3K, 3.6K) AF*-SL (*= 3K, 3.6K, 4K, 4.6K, 5K, 5.5K, 6K)
Rating……………………………..........:	See below Specifications table

Specifications table					
Model	AF1K-SL-1	AF1.5K-SL-1	AF2K-SL-1	AF2.5K-SL-1	AF3K-SL-1
PV input					
P pv Max(W)	1500	2300	3000	3800	4500
Vmax PV (Vdc) (absolute Max.)	550	550	550	550	550
Isc PV (absolute Max.) (A)	26	26	26	26	26
Number MPP trackers	1	1	1	1	1
Number input strings	1	1	1	1	1
Max. PV input current / strings (A)	18.5	18.5	18.5	18.5	18.5
MPPT voltage range (Vdc)	80-500	80-500	80-500	80-500	80-500
Vdc range @ full power (Vdc)	80-500	90-500	120-500	150-500	170-500
Battery (charge/discharge)					
Battery type	Li-ion/Lead-acid				
Battery Normal Voltage (Range) (Vdc)	51.2V (40-60V)				
Max charge/discharge Current(A)	25	40	50	63	80
Max charge/discharge Power(W)	1000	1500	2000	2500	3000
AC Grid (input and output)					
Normal AC Voltage (VAC)	L/N/PE, 230Vac				
Frequency (Hz)	50				
Normal AC Current (A)	4.4	6.6	8.7	10.9	13.1
Max. cont. input/output current (A)	5	7	10	12	14
Rated Power(W)	1000	1500	2000	2500	3000
Rated Apparent Power (VA)	1000	1500	2000	2500	3000
Max. cont. Power (W)	1000	1500	2000	2500	3000
Max. cont. Apparent Power (VA)	1000	1500	2000	2500	3000
Power factor (adjustable)	1.0(-0.8~ +0.8)				
AC Load output (stand alone)					
Normal Voltage (VAC)	L/N/PE, 230Vac				
Frequency (Hz)	50				
Nominal Current(A)	4.4	6.6	8.7	10.9	13.1
Max. cont. current (A)	5	7	10	12	14
Max. cont. Power (W)	1000	1500	2000	2500	3000
Rated Apparent Power (VA)	1000	1500	2000	2500	3000
Max. cont. Apparent Power (VA)	1000	1500	2000	2500	3000
Power factor	1.0				
Others					
Ingress protection (IP)	IP65				
Protective class	Class I				
Temperature (°C)	-25°C to +60°C (Derating >45°C)				
Inverter Isolation	Non-isolated (PV-AC-BAT)				
Overvoltage category	OVC III (AC Main), OVC II (PV)				
Firmware	V06				

Specifications table				
Model	AF3.6K-SL-1	AF3K-SL	AF3.6K-SL	AF4K-SL
PV input				
P pv Max(W)	5400	4500	5400	6000
Vmax PV (Vdc) (absolute Max.)	550	550	550	550
Isc PV (absolute Max.) (A)	26	26 x 2	26 x 2	26 x 2
Number MPP trackers	1	2	2	2
Number input strings	1	1/1	1/1	1/1
Max. PV input current / strings (A)	18.5	18.5 x 2	18.5 x 2	18.5 x 2
MPPT voltage range (Vdc)	80-500	80-500	80-500	80-500
Vdc range @ full power (Vdc)	210-500	90-500	110-500	120-500
Battery (charge/discharge***)***				
Battery type	Li-ion/Lead-acid			
Battery Normal Voltage (Range) (Vdc)	51.2V (40-60V)			
Max charge/discharge Current(A)	80	80	80	80
Max charge/discharge Power(W)	3600	3000	3600	4000
AC Grid (input and output)				
Normal AC Voltage (VAC)	L/N/PE, 230Vac			
Frequency (Hz)	50			
Normal AC Current (A)	15.7	13.1	15.7	17.4
Max. cont. input/output current (A)	17	14	17	19
Normal Power (W)	3600	3000	3600	4000
Rated Apparent Power (VA)	3600	3000	3600	4000
Max. cont. input/output Power (W)	3600	3000	3600	4000
Max. cont. Apparent Power (VA)	3600	3000	3600	4000
Power factor(adjustable)	1.0(-0.8~ +0.8)			
AC Load output (stand alone)				
Normal Voltage (VAC)	L/N/PE, 230Vac			
Frequency (Hz)	50			
Nominal Current (A)	15.7	13.1	15.7	17.4
Max. cont. current (A)	17	14	17	19
Max. cont. Power (W)	3600	3000	3600	4000
Rated Apparent Power (VA)	3600	3000	3600	4000
Max. cont. Apparent Power (VA)	3600	3000	3600	4000
Power factor	1.0			
Others				
Ingress protection (IP)	IP65			
Protective class	Class I			
Temperature (℃)	-25°C to +60°C (Derating >45°C)			
Inverter Isolation	Non-isolated (PV-AC-BAT)			
Overvoltage category	OVC III (AC Main), OVC II (PV)			
Firmware	V06			

Specifications table				
Model	AF4.6K-SL	AF5K-SL	AF5.5K-SL	AF6K-SL
PV input				
P pv Max(W)	6900	7500	8300	9000
Vmax PV (Vdc) (absolute Max.)	550	550	550	550
Isc PV (absolute Max.) (A)	26 x 2	26 x 2	26 x 2	26 x 2
Number MPP trackers	2	2	2	2
Number input strings	1/1	1/1	1/1	1/1
Max. PV input current / strings (A)	18.5 x 2	18.5 x 2	18.5 x 2	18.5 x 2
MPPT voltage range (Vdc)	80-500	80-500	80-500	80-500
Vdc range @ full power (Vdc)	130-500	150-500	160-500	170-500
Battery (charge/discharge)				
Battery type	Li-ion/Lead-acid			
Battery Normal Voltage (Range) (Vdc)	51.2V (40-60V)			
Max charge/discharge Current(A)	80	80	80	80
Max charge/discharge Power(W)	4600	4800	4800	4800
AC Grid (input and output)				
Normal AC Voltage (VAC)	L/N/PE, 230Vac			
Frequency (Hz)	50			
Normal AC Current (A)	20	21.8	24	26.1
Max. cont. input/output current (A)	22	23	26	28
Normal Power (W)	4600	5000	5500	6000
Rated Apparent Power (VA)	4600	5000	5500	6000
Max. cont. input/output Power (W)	4600	5000	5500	6000
Max. cont. Apparent Power (VA)	4600	5000	5500	6000
Power factor(adjustable)	1.0(-0.8~ +0.8)			
AC Load output (stand alone)				
Normal Voltage (VAC)	L/N/PE, 230Vac			
Frequency (Hz)	50			
Nominal Current(A)	20	21.8	24	26.1
Max. cont. current (A)	22	23	26	28
Max. cont. Power (W)	4600	5000	5500	6000
Rated Apparent Power (VA)	4600	5000	5500	6000
Max. cont. Apparent Power (VA)	4600	5000	5500	6000
Power factor	1.0			
Others				
Ingress protection (IP)	IP65			
Protective class	Class I			
Temperature (°C)	-25°C to +60°C (Derating >45°C)			
Inverter Isolation	Non-isolated (PV-AC-BAT)			
Overvoltage category	OVC III (AC Main), OVC II (PV)			
Firmware	V06			

List of attachments
Attachment 1 - Photo Attachment 2 – Test Data

Test item particulars... :

Class of equipment …………………………………:	☐Stand-alone inverter ☐Grid-interactive inverter ☒Multiple mode inverter ☐Charger controller ☒Hybrid Inverter
Connection to the mains..:	☐ pluggable equipment ☐ direct plug-in ☒ permanent connection ☐ for building-in
Equipment mobility ....:	☐movable ☐ hand-held ☐ stationary ☒fixed ☐ transportable ☐ for built-in
Enviromental category ....:	☒outdoor ☐indoor unconditional ☐indoor conditional
Over voltage category Mains.....................................:	☐ OVC I ☐ OVC II ☒OVC III ☐ OVC IV
Over voltage category PV..:	☐ OVC I ☒OVC II ☐ OVC III ☐ OVC IV
Class of equipment..:	☒Class I ☐ Class II ☐ Class III ☐Not classified

Possible test case verdicts:

- test case does not apply to the test object.................:	N/A
- test object does meet the requirement ....:	P(Pass)
- test object does not meet the requirement ....:	F(Fail)

Testing.. :

Date of receipt of test item..:	2022-08-15
Date (s) of performance of tests..................................:	2022-08-29 to 2022-09-23

General remarks:

The test results presented in this report relate only to the object tested.
This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory.

"(see Enclosure #)" refers to additional information appended to the report.
"(see appended table)" refers to a table appended to the report.
Throughout this report a point is used as the decimal separator.

Determination of the test result includes consideration of measurement uncertainty from the test equipment and methods.

Determination of the test conclusion is based on IEC Guide 115 in consideration of measurement uncertainty.

The test results presented in this report relate only to the item tested. The results indicate that the specimen complies with standard" AS/NZS 4777.2: 2020".

General product information:

The unit is non-isolated (transformer-less) hybrid inverter for connection with public low voltage grid.

The Inverter is single-phase type 1φ/N/PE, 230 Vac and non-isolated between PV circuit and AC main circuit, it provides two relays in series on each grid conductor (L, N). The internal control is redundantly built. It contains a MCU and a DSP. Both can open relays independently and communicate with each other.

Block diagram:
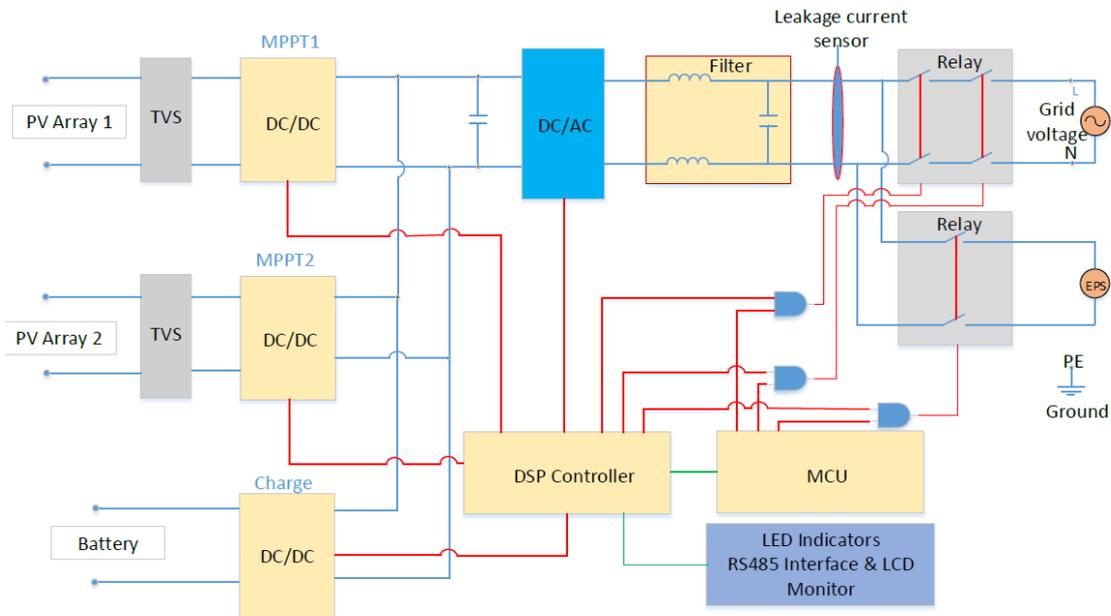
The neutral conductor of EPS port shall be connected to the AC grid after the installation.

Warning:
A type B RCD is required on the EPS port of the inverter.
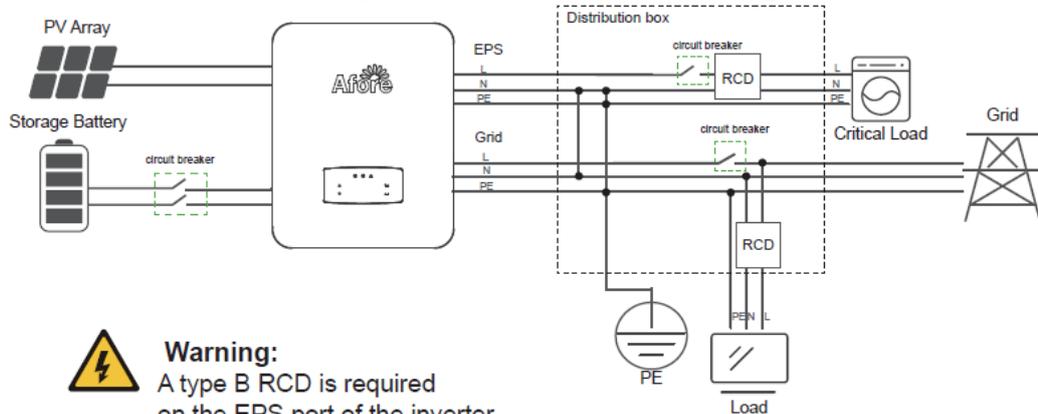
The inverter doesn't need to operate and maintenance after installation.

To protect the PCE, user and installer, external DC and AC circuit breakers shall be equipped at the end use application.

The testing performed on typical model AF6K-SL unless otherwise specified.

The software version used for the testing is:
    DSP: V06
    MCU: V06

Model difference:

All models AF*-SL-1 (*= 1K, 1.5K, 2K, 2.5K, 3K, 3.6K), AF*-SL (*= 3K, 3.6K, 4K, 4.6K, 5K, 5.5K, 6K) have same circuit diagram, PWB layout and software. Only different power ratings by software and quantity of MPP trackers. AF*-SL-1 has 1 MPP tracker, AF*-SL has 2 MPP trackers.

Copy of label

The other model labels are same with above except model number and technical data.

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Mode: AFx-SL

	3K	3.6K	4K	4.6K	5K	5.5K	6K

PV Input

Vpv Max	(V)	550						
Vpv MPPT	(V)	80-500						
Ipv Max	(A)	18.5x2						
Isc Max	(A)	26x2						
Ppv Max	(kW)	4.5	5.4	6	6.9	7.5	8.3	9

Battery

Battery Type		Li-ion/Lead-acid						
Vbat Range	(V)	40-60						
Icc/Idc Max	(A)	80						
Pcc/Pdc Max	(kW)	3	3.6	4	4.6	4.8	4.8	4.8

AC Grid

Vgrid Nom	(V)	230						
fgrid Nom	(Hz)	50						
Igrid Nom	(A)	13.1	15.7	17.4	20	21.8	24	24.1
Igrid Cont.	(A)	14	17	19	22	23	26	28
Pgrid Cont.	(kW)	3	3.6	4	4.6	5	5.5	6
Sgrid Nom	(kVA)	3	3.6	4	4.6	5	5.5	6
Power Factor		1 (-0.8~+0.8 adjustable)						

AC Load Output

VACLoad Nom	(V)	230						
fACLoad Nom	(Hz)	50						
IACLoad Cont.	(A)	14	17	19	22	23	26	28
SACLoad Nom	(kVA)	3	3.6	4	4.6	5	5.5	6
SACLoad Peak	(kVA)	4.5 (10min)	5.4 (10min)	6 (10min)	6.9 (10min)	7.5 (10min)	8.3 (10min)	9 (10min)
Overvoltage category		OVC III (AC Main), OVC II (PV)						
Inverter Isolation		Non-isolated (PV-AC-BAT)						
Protective Class		I						
IP Degree		IP65						
Operating temperature range		-25~+60℃ (Derating 45℃)						

DRM0	DRM1	DRM2	DRM3	DRM4	DRM5	DRM6	DRM7	DRM8
☒	☐	☐	☐	☐	☐	☐	☐	☐

S/N

HL2028-01

RoHS

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WARNING

Hot surfaces
To reduce the risk of burns. Do not touch.

Risk of electric shock
Both AC and DC voltage sources are terminated inside this equipment. Each circuit must be individually disconnected before servicing and when the photovoltaic array is exposed to light, it supplies a DC voltage to this equipment.

Risk of electric shock from energy stored in capacitor. Do not remove cover until 5 minutes after disconnecting all sources of supply.

Risk of electric shock, do not remove cover. No user serviceable parts inside. Refer servicing to qualified service personnel.

Check user manual before service
Refer to the operation instruction.

NO warranty for disassembled inverter
Warranty doesn't provide for the inverter disassembled by non-authorized staff.

WARNING: POWER FED FROM MORE THAN ONE SOURCE
For continued protection against risk of fire, replace only with same type and ratings of fuse.

Series No.

S2260L0012227805

Remark:
1. The other model labels are same with above except model number and technical data.
2. Printed symbols shall be at least 2.75 mm high. Printed text characters shall be at least 1.5 mm high, whether upper case or lower case, and shall contrast in colour with the background.
3. The tenth to thirteenth of the serial number (2132): 21=year 32=week.

AS/NZS 4777.2			
Clause	Requirement – Test	Result - Remark	Verdict
2	GENERAL REQUIREMENTS		P
2.1	General		P
	This Standard does not prevent the use of materials, methods of assembly, procedures, or additional functions and the like that are not specifically included in the requirements of this Standard, or are not mentioned in it, provided the minimum safety, functional and performance requirements specified herein are met.	Considered	P
2.2	Electrical safety		P
	Inverters for use in inverter energy systems with photovoltaic (PV) arrays and/or batteries shall conform to IEC 62109-1 and IEC 62109-2, and the requirements within this Standard. Throughout IEC 62109-1 and IEC 62109-2, the term "power conditioning equipment (PCE)" is used. For the purposes of this Standard, "PCE" shall be replaced with the term "inverter".	See IEC62109-1/-2 report: 220901962SHA-001/002	P
	Inverters for use in inverter energy systems that have energy storage (batteries) as the only possible energy source shall conform to the electrical safety requirements of IEC 62477-1, and the requirements within this Standard. Inverters for use in inverter energy systems that incorporate energy sources other than photovoltaic (PV) arrays or batteries shall conform to IEC 62477-1, and the requirements within this Standard. Throughout IEC 62477-1, the term "power electronic converter system (PECS)" is used. For the purposes of this Standard, "PECS" shall be replaced with the term "inverter". NOTE The application of relevant electrical safety standards for energy source types is under consideration. The requirements of IEC 62477-1, IEC 62109-1 and IEC 62109-2 may be of some use in identifying potential hazard and risk mitigation methods.		N/A
2.3	Provision for external connections		P
2.3.1	General		P
	Inverters shall be used and installed as fixed equipment only. Inverters shall not be used as portable equipment.		P
	Where an inverter is integral within an electric vehicle, the inverter shall be connected in accordance with Clause 2.3.3.2.		N/A
	Inverter provisions for external connection —		P
	a) shall be for fixed equipment only; and	Fixed equipment	P
	b) shall provide for safe and reliable connection to any d.c. source or load or any a.c. source or load.		P
	All inverter ports (except communications ports) shall incorporate connection types for either —		P
	(i) permanently connected equipment (see Clause 2.3.2); or (ii) pluggable type B equipment (see Clause 2.3.3).	Permanently connected equipment	P

	AS/NZS 4777.2		
Clause	Requirement – Test	Result - Remark	Verdict
	Inverter source or load connections shall not incorporate connection types for pluggable type A equipment.		P
2.3.2	Permanently connected equipment		P
	Permanently connected inverters shall have terminals for connection to fixed installation wiring.		P
2.3.3	Pluggable type B equipment		P
2.3.3.1	General		P
	Pluggable type B equipment shall have one of the following means of connection:		P
	(a) A non-detachable cord for connection to the electrical installation by means of a connector.		N/A
	(b) An appliance inlet that can be connected to a matching connector.	PV connector and ac connector used.	P
	Pluggable type B equipment shall not incorporate — (i) a connection by a connector or inlet conforming to any of the dimensional sheets of AS/NZS 60320.1; (ii) a connection by a plug conforming to AS/NZS 3112; or (iii) a connection by a connector or inlet where hazardous voltages are accessible by the standard test finger. NOTE The standard test finger is the same as that used in IEC 62109-1.	Certified PV connector and ac connector used, see IEC 62109-1 report: 220901962SHA-001	P
2.3.3.2	Electric vehicle connections		N/A
	Pluggable type B equipment for an electric vehicle used in an inverter energy system connected via flexible lead with a plug shall —		N/A
	(a) be Mode 3 or Mode 4 in accordance with IEC 61851-1;		N/A
	(b) utilize a Case C connection as per IEC 61851-1 between the fixed electric vehicle supply equipment and the electric vehicle; and		N/A
	(c) utilize connectors that comply with AS IEC 62196.2 in the case of Mode 3 or IEC 62196-3 in the case of Mode 4.		N/A
2.4	Earth fault/earth leakage detection		P
2.4.1	Photovoltaic (PV) array earth fault/earth leakage detection		P
	For inverter energy systems used with PV array systems that require earth fault detection and residual current detection, either internal or external to the inverter, the type of detection used shall be declared in accordance with IEC 62109-1 and IEC 62109-2.	See IEC62109-1/-2 report: 220901962SHA-001/002	P
	If an external residual current device (RCD) is required, the manufacturer's installation instructions shall state the need for an RCD and shall specify its rating, type and required circuit location in accordance with Section 7.		N/A
	Compliance shall be checked by inspection of the inverter's markings and manufacturer's documentation, and testing in accordance with IEC 62109-2.	See IEC62109-2 report: 220901962SHA-002	P
	Where the additional detection for functionally earthed PV arrays, as required by AS/NZS 5033, is present in the inverter, this additional detection shall, before start-up of the system —		P

AS/NZS 4777.2			
Clause	Requirement – Test	Result - Remark	Verdict
	(a) open circuit the functional earth connection to the PV array;		P
	(b) measure the resistance to earth of each conductor of the PV array;		P
	(c) if the earth resistance is above the resistance limit (R_{iso} limit) threshold specified in Table 2.1, the system shall reconnect the functional earth and shall be allowed to start; and	See IEC62109-2 report: 220901962SHA-001	P
	(d) if the earth resistance is equal to or less than the resistance limit (R_{iso} limit) threshold specified in Table 2.1, the inverter shall shut down and initiate an earth fault alarm in accordance with the requirements of IEC 62109-2. NOTE 1 Direct functional earthing of systems is not recommended. Functional earthing via a resistor is a safer option wherever it is possible. NOTE 2 R_{iso} limit is the same as in AS/NZS 5033.	See IEC62109-2 report: 220901962SHA-001	P
2.4.2	Battery Energy Storage System (BESS) earth fault/earth leakage detection		N/A
	For inverters used with battery systems, the requirements for earth fault alarm monitoring of AS/NZS 5139 may apply..		N/A
	Where an inverter has a port for connecting a battery system installation that requires an alarm for monitoring of earth faults in conformance to AS/NZS 5139, the inverter should provide an alarm. Where no alarm is provided in the inverter, the inverter documentation shall require the addition of an external alarm and monitoring device.		N/A
	The inverter documentation should refer to the battery system manufacturer's instructions for earth fault monitoring and earth leakage levels that indicate a fault.		N/A
2.5	Compatibility with electrical installation		P
	The inverter shall be compatible with wiring practices for LV electrical installations of AS/NZS 3000 and variations as required in AS/NZS 4777.1. The inverter a.c. voltage and frequency operation shall conform to the limits specified in AS 60038. NOTE The inverter needs to have a.c. voltage and frequency ratings compatible with Australian and New Zealand electrical supply regulations as a minimum requirement. In Australia, the voltage ranges present on electrical distribution networks may be in accordance with AS 61000.3.100. In New Zealand, the voltage range is specified in Electricity (Safety) Regulations 2010 (NZ) and is less than the limit specified in AS 60038.	See installation manual	P
2.6	Reactive power capability		P

AS/NZS 4777.2		
Clause	Requirement – Test	Result - Remark	Verdict
	The inverter shall be capable of absorbing or supplying at least the specified reactive power of Clause 3.3 down to a power factor of 0.8 for all active power output or input levels above 60 % of rated apparent power. Where the active power output or input level is between 20 % and 60 % of rated apparent power, the inverter shall be capable of absorbing or supplying reactive power of at least 44 % of rated apparent power. Where the active power output or input level is below 20 % of rated apparent power, reactive power being absorbed or supplied may be reduced due to limitation of inverter power factor capabilities. The minimum reactive power capability requirement is shown in Figure 2.1. NOTE For inverter active power output or input below 20 % of rated apparent power, the reactive power may be controlled such that the vars supplied or absorbed are less than the amount of vars supplied or absorbed at 20 % of rated apparent power output or input.	See measurement result	P
2.7	Harmonic currents		P
	The harmonic currents of the inverter shall not exceed the limits specified in Tables 2.2 and 2.3 and the total harmonic current distortion (ITHD) to the 50th harmonic shall be less than 5 %.	See measurement result	P
	Compliance shall be determined by type testing in accordance with the harmonic current limit test specified in Appendix B. NOTE The inverter should not significantly radiate or sink frequencies used for ripple control by the local electrical distributor. The distributor should be consulted to determine which frequencies are used. Fitting of additional filtering components may be required in some grid areas.		P
2.8	Voltage fluctuations and flicker		P
	The inverter shall conform to the voltage fluctuation and flicker limits specified in AS/NZS 61000.3.3 for equipment with rated current less than or equal to 16 A per phase (a.c.).	See measurement result	P
	For equipment with rated current greater than 16 A per phase (a.c.), if the inverter cannot meet the requirements of AS/NZS 61000.3.3, the maximum permissible connection point impedance (Zmax) shall be determined such that the voltage fluctuation and flicker limits specified in AS/NZS 61000.3.3 can be met. The impedance shall be determined in accordance with the methods given in AS/NZS 61000.3.11. The values of P_{st} and P_{lt}, when tested using Z_{ref}, and the network impedance value (Z_{max} or Z_{ref}) required for compliance shall be included in the inverter documentation. NOTE Definitions of P_{st} and P_{lt} and the value of Z_{ref} are given in AS/NZS 61000.3.3.	See measurement result	P
	Compliance shall be determined by testing in accordance with the relevant Standard. The inverter shall remain connected throughout the test and the automatic disconnection device shall not operate.		P
2.9	Transient voltage limits		P

AS/NZS 4777.2		
Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	To prevent damage to electrical equipment connected to the same circuit as the inverter, disconnection of the inverter from the grid shall not result in transient overvoltages beyond the limits specified in Table 2.4.		P
	Compliance shall be determined by type testing in accordance with the transient voltage limit test specified in Appendix C. The voltage-duration curve is derived from the measurements taken at the grid-interactive port of the inverter.	See measurement result	P
	The transient voltage limits listed in Table 2.4 are graphically illustrated in Figure 2.2.		P
2.10	D.C. current injection		P
	In the case of a single-phase inverter, the d.c. current output of the inverter at any a.c. port including the grid-interactive and/or stand-alone port shall not exceed 0.5 % of the inverter's rated current or 5 mA, whichever is the greater.	See measurement result	P
	In the case of a three-phase inverter, the d.c. current output of the inverter at any a.c. port, including the grid-interactive and/or stand-alone port, measured in each of the phases, shall not exceed 0.5 % of the inverter's per-phase rated current or 5 mA, whichever is the greater.		N/A
	If the inverter does not incorporate a mains frequency isolating transformer or is not used with a dedicated external isolation transformer, it shall be type tested to ensure the d.c. current output at any a.c. port of the inverter is below the limits specified above at all current output levels.		P
	Compliance shall be determined by type testing in accordance with the d.c. current injection test specified in Appendix D. NOTE For any inverter capable of injecting d.c. fault current into the electrical installation the selection of an RCD, where required, needs to be such that the RCD operates correctly with the level of d.c. fault current being injected.	See measurement result	P
2.11	Current balance for three-phase inverters		N/A
	In the case of a three-phase inverter the a.c. current output shall be generated and injected into the three-phase electrical installation as a three-phase balanced current.	Single phase inverter	N/A
	Compliance shall be determined by type testing in accordance with the following requirement. The a.c. current output for each phase for three-phase balanced current shall be within 5 % of the measured value of the other phases at rated current when injected into a balanced three-phase voltage.		N/A
	Inverters which can be used in a voltage balance mode, as defined in Clause 3.3.2.4, are allowed to generate unbalanced currents.		N/A
2.12	Isolation of energy sources		P
2.12.1	General		P

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Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	Where an energy source port has a load break switching device that is part of and within the inverter and is part of the method for isolating the energy source, the load break switching device/s shall —		P
	(a) have a voltage rating equal to or greater than the inverter's maximum voltage rating for that port;	600Vdc DC switch used, DC disconnector voltage rating greater than the inverter's maximum voltage 550Vdc.	P
	(b) interrupt all live conductors simultaneously;		P
	(c) be able to be secured in the open position and only secured when the main contacts are in the open position;		P
	(d) be either a switch disconnector that conforms to Clause 2.12.2 or a circuit breaker that conforms to Clause 2.12.3;		P
	(e) conform to additional requirements of Clause 2.12.4 for PV array energy source;		P
	(f) conform to additional requirements of Clause 2.12.5 for battery system energy sources; and	No DC switch disconnector integrated for battery system.	N/A
	(g) for all energy sources other than those listed in Items (e) and (f) be rated for a.c. or d.c. operation per the port type, and if d.c. rated be a non-polarized type.	Non-polarized DC switch disconnector used.	P
	Where a load break switching device is part of and within the inverter, and forms part of the method for isolating the energy source/s, there shall be a warning label to isolate energy source/s prior to removal of any cover for maintenance or repair.	See instruction manual	P
	Documentation of permitted and safe access (including isolation) to inverters for maintenance and repair shall be included in manuals.		P
	Combination fused switch disconnectors or fused circuit breakers shall not be used as the load break switching device as part of or within the inverter.		N/A
	Where any load break switching device is part of and within the inverter and does not meet the requirements of this Clause (2.12.1) a warning label shall be used to indicate that an additional external load break switching device is required. Documentation for an inverter that requires an external load break switching device shall include the requirement of an additional external load break switching device that conforms to the requirements AS/NZS 4777.1. NOTE Use of terminology such as AC-21B, DC-21B, and DC-PV1 are from AS 60947.3.	The integrated DC switch disconnector meet the requirements of clause 2.12.1	P
2.12.2	Switch-disconnector		P
	Where a load break switching device that is part of or within the inverter is a switch-disconnector, it shall —		P
	(a) be rated for independent manual operation;		P
	(b) be classified as suitable for disconnection and be marked with the following symbol: ⎯⎯/⍺⎯		P
	(c) have a utilization category of at least DC-21B where the port is suitable for a d.c. energy source;	DC-PV2	P
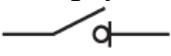
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Clause	Requirement – Test	Result - Remark	Verdict
	(d) have a utilization category at least AC-21B where the port is suitable for an a.c. energy source;		N/A
	(e) conform to relevant switch-disconnector standards as specified for the port and rating criteria in Clauses 2.12.4 or 2.12.5;		P
	(f) have a current rating where rated operational current (Ie) and I(make), and Ic(break) rated current are rated such that the disconnector is capable of interrupting the maximum rated normal and fault current for that port as specified in the inverter documentation; and		P
	(g) have a current rating for the thermal current (Ithe and Ithe solar) rated for the installation environment specified by the manufacturer.		P
2.12.3	Circuit breaker		N/A
	Where a load break switching device that is part of or within the inverter is a circuit breaker, it shall —		N/A
	(a) conform to AS/NZS IEC 60947.2; and		N/A
	(b) be classified as suitable for isolation and be marked with the following symbol:		N/A
2.12.4	PV array ports		P
	For inverters with an apparent power rating of less than 30 kVA the isolating devices for PV array ports that are part of or within the inverter shall conform to the requirements of AS 60947.3 for switch-disconnectors for photovoltaic (PV) d.c. applications.	Certified switch-disconnector used, certificate no. AZ 69026020, issued by TÜV Rheinland Australia Pty Ltd	P
	For inverters with an apparent power rating of 30 kVA or more the isolating devices for PV array ports as a part of or within the inverter shall conform to AS 60947.3 for switch-disconnectors for photovoltaic (PV) d.c. applications with the following modifications:		N/A
	(a) have a minimum utilization category of DC-PV1;		N/A
	(b) for inverters with IP6x or greater, have at least pollution degree 2; and		N/A
	(c) where the utilization category is DC-PV1, have a continuous backfeed current as tested by IEC 62109-1 of less than 0.3 A.		N/A
2.12.5	Battery system ports		N/A
	Isolating devices for battery system ports that are part of or within the inverter shall meet the following additional requirements:		N/A
	(a) Shall conform to AS 60947.3.		N/A
	(b) Shall be of the non-polarized type.		N/A
	(c) Shall have a current rating equal to or greater than the maximum rated d.c. current for the battery system port.		N/A
	(d) Shall have a utilization category of at least DC-21B. NOTE Other d.c. energy ports may be treated the same as a battery system port.		N/A
2.13	Measurement accuracy		P

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Clause	Requirement – Test	Result - Remark	Verdict
	To ensure the stable and reliable operation of the inverter protective functions and all modes of operation, the inverter shall conform to or exceed the measurement and calculation accuracy requirements specified in Table 2.5. Where the inverter utilizes an external measurement device, the measurement and calculation accuracy of the system (including the combination of the inverter and external measurement device) shall conform to the measurement and calculation accuracy requirements specified in Table 2.5.		P
2.14	Prioritization of protection and operational modes		P
	Inverters responding to abnormal voltage or frequency conditions shall meet the prioritization levels of Table 2.6.		P
2.15	Firmware		P
	The inverter firmware determines the functioning of an inverter as well as responses required by this Standard. The functions may be spread over multiple programmable devices. The inverter firmware may change over the life of a specific inverter model.		P
	The inverter firmware version shall be reported in testing. The inverter firmware version identifier shall be accessible for inspection. Inverter firmware version information may be displayed via a panel/screen, external device or software interface.	Firmware version: V06	P
	The inverter firmware shall be secured against inadvertent or unauthorized changes. Changes to the inverter firmware shall require the use of a tool and special instructions not provided to unauthorized personnel. NOTE Special interface devices and passwords are regarded as tools.	Special interface devices shall be used by authorized personnel	P
	Inverter firmware changes and updates shall conform to the requirements of this Standard. Where an inverter firmware update affects any of the provisions specified in Sections 2, 3, 4 and 5 conformance with this Standard shall be determined.		P
3	Operational modes and multiple mode inverters		P
3.1	General		P
	Unless otherwise stated, the modes in the following Clauses are for the grid-interactive port of the inverter.		P
3.2	Inverter demand response modes (DRMs)		P
3.2.1	The inverter shall support the demand response mode DRM 0 of Table 3.1. The inverter should support the other demand response modes of Table 3.1. NOTE 1 The only mandatory demand response mode is DRM 0. Support for other demand response modes is optional.		P
	The inverter shall detect and initiate a response to all supported demand response commands within 2 s. The inverter shall continue to respond while the mode remains asserted.		P
	The inverter shall conform to the relevant requirements of Section 2 and this Section (3), and with all of the requirements of Section 4, while any demand response mode is asserted and following the cessation of a demand response command.		P

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Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	The inverter shall be capable of responding to demand response commands via a demand response enabling device (DRED) as defined in Clause 3.2.2.		P
	Compliance shall be determined by testing as specified in Appendix E. NOTE 2 The demand response modes may be provided via an integrated device or an external device, where DRM 0 meets the requirements of Clause 4.1. Only integrated devices and external devices providing DRM 0 are applicable for testing in this Standard.		P
3.2.2	Interaction with demand response enabling device (DRED)		P
	The inverter shall have a means of connecting to a DRED. This means of connection shall include a terminal block or RJ45 socket. The terminal block or RJ45 socket shall conform to the minimum electrical specifications in Table 3.2. The terminal block or RJ45 socket may be physically mounted in the inverter or in a separate device that remotely communicates with the inverter. NOTE 1 In the absence of a DRED, the inverter may be fitted with a DRED bypass device. NOTE 2 RJ45 is the common name for the 8P8C modular connector specified in ISO/IEC 8877, which is generally used to terminate communications cables. NOTE 3 Where a separate device that remotely communicates with the inverter is used then other methods are possible using a range of different communications systems and protocols in the inverter or external. Provided that this still allows the inverter to interact with the DRED.	RJ45 socket used.	P
	The DRED asserts demand response modes by shorting together terminals or pins as specified in Table 3.3. In detecting the state of the DRED, the inverter shall conform to the following requirements:		P

	(a) The inverter shall not inject more than 30 mA (d.c. or a.c.) into —
	  (i) terminals "DRM1/5", "DRM2/6", "DRM3/7" or "DRM4/8", where a terminal block is used; or
	  (ii) pins 1, 2, 3 or 4, where an RJ45 socket is used.
		See measurement result	P

	(b) The inverter shall allow for a drop of up to 1.6 V across the DRED and associated wiring when nominally shorted.	See measurement result	P
	(c) The inverter shall not supply more than 34.5 V (d.c. or a.c.) to any terminal of the terminal block or RJ45 socket.		P
	(d) If the impedance between pins 5 and 6 is detected to be above 20 kΩ, the inverter shall fail-safe to DRM 0 asserted.	Considered	P
	The RJ45 socket pin assignments for demand response modes are as specified in Table 3.4.		P
	The DRED may assert more than one DRM at a time, in which case the requirements of every active DRM that is supported by the inverter shall be simultaneously satisfied.		P
	The inverter shall detect the assertion of any combination of DRMs which result in terminal 5 and 6 being shorted simultaneously as assertion of DRM 0.		P
	Where DRM 3 or DRM 7 are supported, the reactive power set-point shall be set by default to operate at unity power factor. The reactive power set-point should be adjustable up to a minimum of 60 % of the inverter's kVA rating.		N/A
	The inverter may provide a power supply for use by the DRED. If included this shall be d.c. and of a voltage less than 34.5 V.		P

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Clause	Requirement – Test	Result - Remark	Verdict
	Where an RJ45 socket is used, pins 7 and 8 may be utilized as positive and negative DRED power supply pins respectively. The power supply shall be capable of delivering at least 0.5 A at a minimum of 6 V d.c., otherwise the inverter shall short pins 7 and 8 together.		P
	Where a terminal block is used, only those terminals needed for the supported DRMs are required.		N/A
3.3	Inverter power quality response modes		P
3.3.1	General		P
	The inverter shall have the following power quality response modes:		P
	(a) Volt-var response mode (Clause 3.3.2).		P
	(b) Volt-watt response mode (Clause 3.3.2).		P
	(c) Fixed power factor (Clause 3.3.3).		P
	(d) Reactive power mode (Clause 3.3.3).		P
	(e) Power rate limit (Clause 3.3.4).		P
	The inverter may have the Voltage balance mode (Clause 3.3.2.4).	No such mode	N/A
	For each of the power quality response modes available in the inverter, the inverter shall conform to the relevant requirements of this Section (3) and Section 2, and all of the requirements of Sections 4 and 5, when these modes are enabled or disabled.		P
	Compliance shall be determined by type testing as specified in Appendix F, Appendix G and Appendix J.	See measurement result	P
	If these power quality response modes of operation are controlled by an external device, the external device shall not interfere with the inverter conforming to the relevant requirements of this Section (3) and Section 2, and all of the requirements of Section 4 and 5, when the external device is controlling these modes.	See measurement result	P
	The required characteristics of the power quality response modes are specified below in Clauses 3.3.2, 3.3.3 and 3.3.4. NOTE Additional requirements in Clause 3.4.3 are for multiple mode inverters with energy storage and when operating in charging modes.		P
3.3.2	Volt response modes		P
3.3.2.1	General		P
	The volt–watt and volt–var response modes specified in Clause 3.3.2.2 and Clause 3.3.2.3 shall be able to operate concurrently when both modes are active.		P
	For three-phase inverters, the inverter shall use the average of the three single-phase voltages as the reference voltage to determine the corresponding volt response action.	Not three-phase inverter	N/A
	The volt-watt mode (Clause 3.3.2.2) may be used with the volt-var mode (Clause 3.3.2.3), fixed power factor mode (Clause 3.3.3), or fixed reactive power mode (Clause 3.3.3).		P
	The volt-var mode may be used with the volt-watt mode (Clause 3.3.2.2).		P

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Clause	Requirement – Test	Result - Remark	Verdict
	Where a power quality response mode is enabled the inverter shall commence and complete the required response according to the defined characteristics of Clause 3.3.2 within the relevant times specified in Table 3.5, starting from the time the voltage is measured as deviating by 1 V from the 10 s average. Response times faster than the maximum times in Table 3.5 are permitted, and commencement and completion of the inverter response should not be unnecessarily delayed or slowed.		P
	Compliance shall be determined by type testing in accordance with the power quality (voltage) response mode tests specified in Appendix G.		P
3.3.2.2	Volt–watt response mode		P
	The volt–watt response mode varies the maximum active power output level of the inverter in response to the voltage at its grid-interactive port. The volt–watt response mode shall be enabled by default.		P
	The response curve required for the volt–watt response mode is defined by two volt response reference values and corresponding maximum active power output levels, the default values are listed in Table 3.6. Above V_{W2}, the maximum active power output shall not exceed the limit specified at V_{W2}. An example volt-watt response mode is shown in Figure 3.1.		P
3.3.2.3	Volt–var response mode		P
	The volt–var response mode varies the reactive power absorbed or supplied by the inverter in response to the voltage at its grid-interactive port. The volt–var response mode shall be enabled by default.		P
	The response curve required for the volt–var response is defined by four volt response reference values and corresponding reactive power levels, the default values are listed in Table 3.7. Below V_{V1}, reactive power shall be maintained at the level specified for V_{V1}. Above V_{V4}, reactive power shall be maintained at the level specified for V_{V4}. An example volt-var response mode is shown in Figure 3.2.		P
	Where the inverter apparent power rating is reached, active power level shall be reduced to stay within the inverter apparent power rating while meeting the volt-var mode reactive power requirements of this Clause (3.3.2.3). This behaviour is intended to provide reactive power priority.		P
3.3.2.4	Voltage balance modes	No such mode	N/A
	A voltage imbalance between phases may occur in an electrical installation that presents a load that is not balanced across the phases. Three-phase inverters, or single-phase inverters used in a three-phase combination may be used for voltage balancing between phases by injecting unbalanced three-phase currents into the electrical installation.		N/A
	If the voltage balance mode is available, the following requirements apply:		N/A
	(a) The voltage balance mode shall be disabled by default.		N/A
	(b) For single-phase inverters used in a three-phase combination, the requirements of Clause 5.2 apply.		N/A

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Clause	Requirement – Test	Result - Remark	Verdict
	(c) The voltage balance mode shall be able to —		N/A
	(i) operate correctly with a single fault applied to the voltage balance control system; (ii) detect the fault or loss of operability and cause the inverter to revert to injecting current into the three-phase electrical installation as a three-phase balanced current; or (iii) detect the fault or loss of operability and disconnect the inverter from the electrical installation.		N/A
3.3.3	Fixed power factor mode and reactive power mode		P
	The fixed power factor mode or the reactive power mode may be enabled in some situations by the electrical distributor to meet local grid requirements, one of these modes shall be enabled if the volt-var mode is disabled. These modes shall be disabled by default.		P
	For the fixed power factor mode, the minimum range of settings shall be 0.8 to 1.0 supplying reactive power, and 1.0 to 0.8 absorbing reactive power, the default power factor setting shall be 1.0. The fixed power factor mode is for control of the displacement power factor over the range of inverter power output.		P
	The volt–watt mode and fixed power factor mode shall be able to operate concurrently.		P
	For the fixed power factor mode, the measurement of power factor shall be the displacement power factor of the inverter treated as a load from the perspective of the grid.		P
	For the reactive power mode, the minimum setting range for ratio of reactive power (vars) to rated apparent power shall be at least 60 % absorbing to 60 % supplying, the default reactive power setting shall be 0 %.		P
	The volt–watt mode and reactive power mode shall be able to operate concurrently.		P
	Where the inverter apparent power rating is reached, active power output level shall be reduced to meet the inverter apparent power rating while meeting the fixed power factor mode or reactive power requirements of this Clause (3.3.3). This behaviour is intended to provide reactive power priority. NOTE Refer to Clause 2.6 for reactive power capability.		P
	Compliance shall be determined by type testing in accordance with the fixed power factor mode and reactive power mode test specified in Appendix F.	See test data	P
3.3.4	Power rate limit		P
3.3.4.1	General		P
	The power rate limit for an inverter is a power quality response mode. The inverter shall have the capability to rate limit changes in power generation through the grid-interactive port. Inverters capable of multiple mode operation shall have the capability to rate limit changes in power level (for example increasing/decreasing of charging rates of connected energy storage).		P
	The power rate limit only applies to the changes in power level specified in Clause 3.3.4.3.		P

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Clause	Requirement – Test	Result - Remark	Verdict
	The power rate limit does not apply when the automatic disconnection device is required to operate (i.e. to disconnect). NOTE The power rate limit causes the inverter power level to either ramp up or ramp down smoothly as it transitions from one power level to another. Changes in power level may be constrained by several factors such as the type of energy source connected, energy storage and operating state of the inverter. For example, an inverter without energy storage may not be able to ramp down when required if the energy source ceases suddenly or conversely may not be able to ramp up if the energy source is not able to deliver more power. Likewise, when the inverter is generating maximum power, it can ramp down but cannot ramp up, while a multiple mode inverter with a completely charged storage system may ramp up (discharge power) but cannot ramp up consumption of power (charge power).		P
	Compliance shall be determined by type testing in accordance with the reconnection test specified in Appendix I and the sustained operation for frequency disturbance test in Appendix J.		P
3.3.4.2	Gradient of power rate limit		P
	The power rate limit (WGra) is the ramp rate of active power output in response to changes in power and is defined as a percentage of rated power per minute. The nominal ramp time (Tn) is the nominal time for a 100 % change in power output with a power rate limit of WGra. An inverter shall have an adjustable power rate limit (WGra) which limits the change in power output to the set power rate limit. The default setting for the power rate limit (WGra) for increase and decrease shall be 16.67 % of rated power per minute which is a nominal ramp time of 6 min. $$W_{Gra} = \frac{100\ \%}{T_n}$$		P
	The power rate limit (WGra) shall be adjustable within the range 5 % to 100 % of rated power per minute. It is permitted to have two separate power rate limits for increase and decrease in power level, as follows:		P
	(a) to rate limit an increase in power (W_{Gra+}); and		P
	(b) to rate limit a decrease in power (W_{Gra-}).		P
	The default setting of W_{Gra+} and W_{Gra-} shall be the same as W_{Gra}.	16.67%Pn/min	P
3.3.4.3	Power rate limit modes		P
3.3.4.3.1	General		P
	The inverter power rate limit (WGra) is applicable to operate in the following modes:		P
	(a) Soft ramp up after connect, reconnect or soft ramp up/down following a response to frequency disturbance.		P
	(b) Changes in a.c. operation and control.		P
	(c) Changes in energy source operation.		P
	The following clauses provide operation information for each mode.		P
3.3.4.3.2	Soft ramp up after connect, reconnect or soft ramp up/down following a response to frequency disturbance		P

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Clause	Requirement – Test	Result - Remark	Verdict
	All inverters shall have this mode. This mode shall be enabled as per Clause 4.7 and for the change in power required by Clause 4.5.3 after frequency has been restored to within the required limits.		P
3.3.4.3.3	Changes in a.c. operation and control		P
	If available, this mode shall be enabled for a change in a demand response mode of Clause 3.2 (except for DRM 0). When a demand response mode of Clause 3.2 (except for DRM 0) is asserted or unasserted the power rate limit (WGra) shall apply to the increase or decrease in power generation or consumption and the transitions between power levels. NOTE Changes in DRM modes (except for DRM 0) are dependent on the availability of the energy source or energy storage to respond. For example an increase in power is not possible if the required increase cannot be met by the available energy resource situation.		P
3.3.4.3.4	Changes in energy source operation		P
	This mode only applies to multiple mode inverters with energy storage. It operates when there is a change in the energy resource available to the inverter, which causes a change in power through the grid-interactive port. For this mode the power rate limit (WGra) should apply to the increase or decrease in power generation or consumption, and to the transitions between power levels. For this mode, the power rate limit (WGra) should be able to be enabled or disabled. The power rate limit shall be disabled by default. The increase or decrease for transitions between power levels is contingent on external situations (such as amount of available solar energy, wind energy or discharge capacity). Only for increases or decreases in the power level which are faster than the power rate limit (WGra) does a control action to limit the ramp rate apply.		P
3.3.4.4	Nonlinearity of power rate limit changes		P
	The nonlinearity (NL) of the power rate limit (WGra) in response to a change of the inverter power level, as defined by the characteristic curve depicted in Figure 3.3, shall be less than 10 %.		P
	The following equation shall be used to calculate the maximum nonlinearity: $$NL = \frac{(100 \times \Delta)}{T_n}$$		P
3.4	Multiple mode inverter operation		P
3.4.1	General		P
	The requirements in this Clause for multiple mode inverters are in addition to the requirements for inverters.		P
	Multiple mode inverters operating in charging mode through the grid-interactive port shall conform to the requirements of Clause 3.3.2.3.		P
	When the multiple mode inverter is operating in stand-alone mode and disconnected from the grid all active conductors of the stand-alone port shall be isolated from the grid.		P

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Clause	Requirement – Test	Result - Remark	Verdict
	Multiple mode inverters in stand-alone mode may utilize the grid-interactive port as the stand-alone port or may utilize a separate stand-alone port.		P
	Multiple mode inverters shall be arranged to ensure that the continuity of the neutral conductor to the load from the electrical installation is not interrupted when the inverter is operating in stand-alone mode, disconnected from the grid and supplies a load via the stand-alone port. NOTE The requirements for the automatic disconnection device in Clause 4.2 are intended to ensure that at least basic insulation or simple separation is maintained between the energy source port, the grid-interactive port and stand-alone ports when the inverter ceases to operate.	The neutral conductor of EPS port shall be connected to the AC grid after the installation. See instruction manual for detail.	P
	Multiple mode inverters shall be arranged such that only the allowed installation methods of AS/NZS 3000 and AS/NZS 4777.1 can be used.		P
	When the multiple mode inverter is operating in stand-alone mode and is disconnected from the grid, the stand-alone port shall conform to the requirements for d.c. current injection (refer to Clause 2.10) into the connected load circuits. The type of RCD compatible with and for use on the stand-alone mode outputs shall be declared.		P
3.4.2	Sinusoidal output in stand-alone mode		P
	The a.c. output voltage waveform of a stand-alone port of a multiple mode inverter operating in stand-alone mode, shall conform to the requirements of this Clause (3.4.2). The a.c. output voltage waveform of a stand-alone mode shall have a voltage total harmonic distortion (THD) not exceeding of 5 % and no individual harmonic at a level exceeding 5 %.		P
	Compliance shall be checked by measuring the THD and the individual harmonic voltages with the inverter delivering 5 % power or the lowest continuous available power output greater than 5 %, and 50 % and 100 % of its continuous rated power, into a resistive load, with the inverter supplied with nominal d.c. input voltage. The THD measuring instrument shall measure the sum of the harmonics from n = 2 to n = 50 as a percentage of the fundamental (n = 1) component at each load level.	See appendix table	P
3.4.3	Volt–watt response mode for inverters with energy storage when charging		P
	The volt–watt response mode for charging of energy storage varies the maximum active power input of the inverter from the grid in response to the voltage at its grid-interactive port. An inverter with energy storage that can be charged through the grid-interactive port shall have this volt–watt response mode. This volt–watt response mode is only active when energy storage charges through the grid-interactive port. The volt–watt response mode for charging of energy storage shall be enabled by default.		P
	The response curve required for the volt–watt response is defined by two volt response reference values and corresponding maximum power input levels through the grid-interactive port, the default values are listed in Table 3.8. Example response modes are shown in Figure 3.4.		P

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Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	The inverter shall commence and complete any required volt-watt response for charging according to the defined characteristics of this Clause 3.4.3 within the relevant times specified in Table 3.5.		P
3.4.4	Stand-alone inverters	Not stand-alone inverter	N/A
	There are a variety of stand-alone inverters, which are intended for supply of 230 V a.c. power to loads within the electrical installation only, with energy provided from batteries, solar arrays and/or other d.c. sources. These inverters have a stand-alone port for supplying the loads within the electrical installation separate to the a.c. input port. These inverters also have an a.c. input port that can be directly connected to either a grid or an independent a.c. energy source such as a diesel generating set. A stand-alone inverter is a type of multiple mode inverter.		N/A
	Any inverter that is not a grid-interactive inverter but is an uninterruptible power system (UPS) that is in accordance with AS 62040.1, AS IEC 62040.2, AS IEC 62040.3 and IEC 62040 series is not considered a stand-alone inverter for the purposes of this Standard.		N/A
	The a.c. input port of a stand-alone inverter, means a port provided to support the energy source, such as —		N/A
	(a) charging the system batteries when other energy sources are unavailable;		N/A
	(b) providing direct supply to site loads, bypassing the inverter completely, when local generation such as from solar and batteries is insufficient; or		N/A
	(c) providing supplementary supply to site loads (in parallel with the inverter output) when local generation is insufficient to supply the entire load.		N/A
	Stand-alone inverters shall not output power from the a.c. input port during normal operation or fault conditions.		N/A
	The stand-alone port of a stand-alone inverter shall be separate to the a.c. input port.		N/A
	Where the a.c. input port can be connected to the grid the inverter shall have settings to conform to this Standard for connection to the grid.		N/A
	A stand-alone inverter with an a.c. input port that is connected to a grid, shall conform to the requirements of this Standard with modifications as described in Appendix M. NOTE The arrangement covered by this Clause is for where the a.c. input will use the grid as an alternative/back up energy source for the stand-alone system to supply energy to the installation.		N/A
3.5	Security of operational settings		P
	The settings of the demand response or power quality response modes of the inverter shall be secured against inadvertent or unauthorized change. Changes to the settings shall require the use of a tool and special instructions not provided to unauthorized personnel. NOTE Special interface devices and passwords are regarded as tools.	Considered. Password needed if setting changed, please see Appendix1 Photos.	P
	The settings shall be capable of only being adjusted within the values specified in this Section (3).	Considered.	P
	Compliance shall be determined by inspection.	Considered.	P

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Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	The inverter settings shall be able to be viewed in read-only mode for verification. A set of operational instructions for viewing inverter regional setting shall be available. Inverter operational settings information may be displayed via a panel/screen, external device, or software interface.	Considered.	P
4	Protective functions for connection to electrical installations and the grid		P
4.1	General		P
	There shall be an automatic disconnection device to prevent injection of energy into the point of supply and prevent the formation of an unintentional island with the grid or part thereof when supply from the grid is disrupted. NOTE This includes preventing the formation of an island within any part of the electrical installation, which is normally connected to the grid.		P
	The automatic disconnection device shall operate —		P
	(a) if supply from the grid is disrupted;		P
	(b) when the grid goes outside preset limits (e.g. undervoltage/overvoltage, under-frequency/over-frequency); or		P
	(c) when the demand response mode DRM 0 (see Clause 3.2) is asserted.		P
	For inverter energy systems connected to multiple phases the automatic disconnection device shall operate if any of the above conditions is met on any phase.	Not multiple phases inverter	N/A
	The automatic disconnection device may be within the inverter or a separate device.	Automatic disconnection within the inverter	P
	Compliance shall be determined by type testing the automatic disconnection device within the inverter or combined with the inverter. Where the automatic disconnection device is separate to the inverter (or inverters), the inverter (or inverters) and the automatic disconnection device shall be tested together as though they are one inverter. Compliance of one combination of inverter and automatic disconnection device does not ensure compliance of either device as part of a different combination. Specific requirements are specified in Clauses 4.2 to 4.8.	See test data	P
4.2	Automatic disconnection device		P
	The automatic disconnection device shall prevent power (both a.c. and d.c.) from entering the grid when the automatic disconnection device operates.		P
	The automatic disconnection device shall provide isolation in all live conductors. NOTE 1 The automatic disconnection device need not disconnect sensing and control circuits.		P
	Automatic disconnection devices for isolation shall conform to the following requirements:		P
	(a) They shall be capable of withstanding an impulse voltage for at least over voltage category III and have an adequate contact gap.	Impulse voltage test was performed. Min. gap of relay contact: 2.0mm. see IEC62109-1 report no. 220901962SHA-001	P

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Clause	Requirement – Test	Result - Remark	Verdict
	(b) They shall not be able to falsely indicate that the contacts are open.		P
	(c) They shall be designed and installed so as to prevent unintentional closure, such as might be caused by impact, vibration or the like.		P
	(d) They shall be devices that disconnect all live conductors (active and neutral) of the inverter from the grid-interactive port. *Exception: For multiple mode inverters with stand-alone mode, which conform to IEC 62477.1 , the automatic disconnection device for isolation shall be a device that disconnects active conductors of the multiple mode inverter from the grid-interactive port.*	Two relays connected in series on each active and neutral conductor.	P
	(e) They shall be such that with a single fault applied to the automatic disconnection device or to any other location in the inverter, at least basic insulation or simple separation is maintained between the energy source port and the grid-interactive port when the means of disconnection is intended to be in the open state.	See IEC 62109-2 report: 220901962SHA-002	P
	(f) They shall be such that with a single fault applied to the automatic disconnection device or any other location in the inverter, power is prevented from entering the grid. NOTE 2 In the case of a non-isolated inverter, the prevention of power entering the grid can be achieved by two mechanical automatic disconnection devices in series in each live conductor. In the case of an isolated inverter, the prevention of power entering the grid can be achieved by a single mechanical automatic disconnection device and a semiconductor device (or semiconductor devices) in each live conductor. The control of the two automatic disconnection devices can be achieved by two independent control circuits to satisfy the single fault requirements in Items (e) and (f) consistent with principals of IEC 62109-2.	See IEC 62109-2 report: 220901962SHA-002	P
	The automatic disconnection device shall be capable of interrupting at least the rated current.		P
	A semiconductor (solid-state) device shall not be used for isolation purposes.	Two relays used on each Line and Neutral	P
4.3	Active anti-islanding protection		P
	The combination of the inverter and the automatic disconnection device shall incorporate at least one method of active anti-islanding protection. NOTE 1 Examples of such methods include — (a) shifting the frequency of the inverter away from nominal conditions in the absence of a reference frequency (frequency shift); (b) allowing the frequency of the inverter to be inherently unstable in the absence of a reference frequency (frequency instability); (c) periodically varying the power output of the inverter (power variation); and (d) monitoring for sudden changes in the impedance of the grid by periodically injecting a current pulse (current injection).	Frequency shift used	P
	The method used to provide active anti-islanding protection shall be declared in documentation. NOTE 2 Active anti-islanding protection is required in addition to the passive anti-islanding protection specified in Clause 4.4 to prevent a situation where islanding may occur because multiple inverters and/or other generators are providing a frequency and voltage reference for one another and/or because load and generation is balanced.		P
	To prevent islanding, the active anti-islanding protection system shall operate the automatic disconnection device (see Clause 4.2) within 2 s of disruption to the power supply from the grid.	See test data	P

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Clause	Requirement – Test	Result - Remark	Verdict
	Compliance shall be determined by type testing in accordance with the active anti-islanding test specified in Appendix H.	See test data	P
4.4	Voltage and frequency limits (passive anti-islanding protection)		P
	The combination of the inverter and the automatic disconnection device shall incorporate the following forms of passive anti-islanding protection:		P
	(a) Undervoltage and overvoltage protection. (b) Under-frequency and over-frequency protection.		P
	For sustained variation of the voltage and frequency beyond each limit specified in Table 4.1 and Table 4.2, the automatic disconnection device (see Clause 4.2) shall operate no sooner than the required trip delay time and before the maximum disconnection time.		P
	The inverter shall remain in continuous operation for voltage and frequency variations with a duration shorter than the trip delay time specified in Table 4.1 and Table 4.2. The inverter shall remain in continuous operation and operate, as required by Clauses 4.5.4, 4.5.5 and 4.5.6, for voltage and frequency variations with a duration shorter than the trip delay time specified in Table 4.1 and Table 4.2.		P
	Each protective function limit shall be preset and secured against change on selection of the specific region.		P
	For a multiple mode inverter meeting the performance classification for output requirements of AS IEC 62040.3 that provides an operational mode to supply load continuously during grid disruption, the inverter may disconnect the grid-interactive port within the trip delay time, provided that when the grid voltage recovers within the voltage requirements of the AS IEC 62040.3 performance classification within the trip delay time the inverter shall reconnect within 400 ms.		N/A
	Compliance shall be determined by type testing in accordance with the voltage and frequency limits tests specified in Appendix I.	See test data	P
4.5	Limits for sustained operation		P
4.5.1	General		P
	The inverter or inverter energy system shall remain in continuous operation over the range of voltages and frequencies that it is required to be compatible with. Refer to Clause 2.5.		P
4.5.2	Sustained operation for voltage variations		P
	The inverter shall operate the automatic disconnection device (see Clause 4.2) within 3 s when the average voltage for a 10 min period exceeds the Vnom-max specified in Table 4.3.		P
	The sustained operation for voltage variations shall not interfere with the active and passive anti-islanding requirements of Clauses 4.3 and 4.4.		P
	The 10 min average value shall be compared against the limit Vnom-max at least every 3 s to determine when to disconnect. NOTE The 10 min average value needs to be calculated for the preceding 10 min based on measurements at the inverter's terminals.		P

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Clause	Requirement – Test	Result - Remark	Verdict
	Compliance shall be determined by type testing in accordance with the sustained operation for voltage variations test specified in Appendix J.		P
4.5.3	Sustained operation for frequency variations		P
4.5.3.1	General		P
	The inverter shall be capable of supplying rated power between 45 Hz and 52 Hz.		P
	Where the inverter is a multiple mode inverter connecting an energy storage system it shall be capable of charging the energy storage from the grid-interactive port between 49.5 Hz and 55 Hz.		P
	The inverter shall maintain continuous operation for frequency variations within the limits specified in Table 4.4 and respond as defined in Table 4.5.		P
	Where a frequency variation results in frequency to be outside the continuous operation range, the inverter shall respond according to the defined characteristics of Clause 4.5.3.2 and Clause 4.5.3.3.		P
	The inverter shall commence its response within the specified time of Table 4.6, starting from the time the frequency is measured as crossing the continuous operation threshold (either f_{LLco} or f_{ULco}). The inverter shall complete its response within the specified time of Table 4.6, starting from the time the frequency reaches its maximum deviation. Response time faster than the maximum times in Table 4.6 are permitted, and commencement and completion of the inverter response should not be unnecessarily delayed or slowed.	See test data	P
	Where a frequency variation results in a change of power level of an inverter, the inverter power shall remain at the required level, until the frequency is maintained within the continuous operating region (less the hysteresis margin) for a period of 20 s. Table 4.7 provides values for hysteresis margin (f_{hyst}) for each region.	See test data	P
	When the conditions for returning to continuous operation defined in Clause 4.5.3.2 and 4.5.3.3 have been met, any change in power level shall be at a rate no greater than the power rate limit (W_{Gra}) of Clause 3.3.4.	See test data	P
	Compliance shall be determined by type testing in accordance with the sustained operation for frequency variations test specified in Appendix J.	See test data	P
4.5.3.2	Response to a decrease in frequency		P
4.5.3.2.1	General response to a decrease in frequency		P
	The inverter shall not reduce power output through the grid-interactive port in response to a decrease in frequency.		P
	In addition, when a disturbance results in a decrease in frequency below the continuous operation range (f_{LLco}) and where the inverter has a reduced output due to a power quality response mode or demand response mode, the inverter shall increase the power output linearly with the decrease in frequency until the lower limit frequency range (f_{Pmax}) is reached.	See test data	P

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Clause	Requirement – Test	Result - Remark	Verdict
	The power output level present at the time the frequency falls below f_{LLCO} shall be held as the reference power output level used to calculate the required response to the decrease in frequency.	See test data	P
	This is expressed in the equation below: $$P_{out} = P_{ref} + \left[(P_{max} - P_{ref}) \left(\frac{(f_{LLCO} - f)}{(f_{LLCO} - f_{Pmax})} \right) \right]$$		P
	When the frequency equals f_{Pmax} the inverter power output level shall be the maximum power output level (P_{max}). The power output level reached may be limited by the energy source availability.	See test data	P
	The inverter power output level shall remain at or above the highest power output level reached in response to the decrease in frequency between f_{LLCO} and f_{Pmax}. This is to provide hysteresis in the control of the inverter. When the frequency has increased above ($f_{LLCO} + f_{hyst}$) for at least 20 s, the inverter shall return to continuous operation. Any change in power output level shall be at a rate no greater than the power rate limit (W_{Gra}) of Clause 3.3.4.	See test data	P
4.5.3.2.2	Response to a decrease in frequency for multiple mode inverters with energy storage	See test data	P
	The response to a decrease in frequency for multiple mode inverters with energy storage is a two-stage response. The initial stage applies if the energy storage is being charged via the grid-interactive port of the inverter and requires a reduction in the power input level through the grid-interactive port, the second stage requires the inverter to increase power output through the grid-interactive port as the frequency continues to decrease.		P
	When a disturbance results in a decrease in frequency that falls below the continuous operation range (f_{LLCO}), and where the multiple mode is generating through the grid-interactive port (from any energy source) it shall maintain at least the same power output level until $f_{stop-ch}$.		P
	When a disturbance results in a decrease in frequency that falls below the continuous operation range (f_{LLCO}), and where the multiple mode inverter is charging the energy storage from the grid-interactive port it shall reduce the power input level linearly with the decrease in frequency until $f_{stop-ch}$ is reached.		P
	The power input level present at the time the frequency falls below f_{LLCO} shall be held as the reference power level used to calculate the required response to the decrease in frequency.		P
	The required response is expressed in the equation below: $$P_{charge} = P_{ref-ch} \left[1 - \frac{(f_{LLCO} - f)}{(f_{LLCO} - f_{stop-ch})} \right]$$		P
	When the frequency falls below $f_{stop-ch}$, the inverter shall have ceased charging the energy storage via the grid-interactive port (i.e. 0 W).		P

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Clause	Requirement – Test	Result - Remark	Verdict
	When a disturbance results in a decrease in frequency that falls below $f_{stop\text{-}ch}$ the multiple mode inverter with energy storage shall increase the power output level through the grid-interactive port linearly with the decrease in frequency until f_{Pmax} is reached, the maximum discharge rate of the energy storage is reached, or the state of charge of the energy storage is exhausted.		P
	The required response is expressed in the equation below: $$P_{\text{out}} = \begin{cases} P_{\max}\left[\dfrac{(f_{\text{stop-ch}} - f)}{(f_{\text{stop-ch}} - f_{\text{Pmax}})}\right] & \text{if inverter charging before disturbance} \\ P_{\text{ref}} + (P_{\max} - P_{\text{ref}})\left[\dfrac{(f_{\text{stop-ch}} - f)}{(f_{\text{stop-ch}} - f_{\text{Pmax}})}\right] & \text{if inverter generating before disturbance} \end{cases}$$		P
	The inverter power level shall remain —		P
	(a) at or below the lowest power input level reached in response to the decrease in frequency between f_{LLCO} and $f_{stop\text{-}ch}$; or (b) at or above the highest power output level reached in response to the decrease in frequency between $f_{stop\text{-}ch}$ and f_{Pmax} (unless the state of charge of the energy storage is exhausted).		P
	When the frequency has increased above ($f_{LLCO}+f_{hyst}$) for at least 20 s, the inverter shall be returned to continuous operation. This is to provide hysteresis in the control of the inverter. Any change in power level shall be at a rate no greater than the power rate limit (W_{Gra}) of Clause 3.3.4.		P
4.5.3.3	Response to an increase in frequency		P
4.5.3.3.1	General response to an increase in frequency	See test data	P
	When a disturbance results in an increase in frequency that exceeds the continuous operation range (f_{ULCO}), the inverter shall reduce the power output linearly with the increase in frequency until f_{Pmin} is reached.		P
	The power output level present at the time the frequency exceeds f_{ULCO} shall be held as the reference power level used to calculate the required response to the increase in frequency.		P
	This is expressed in the equation below: $$P_{\text{out}} = P_{\text{ref}}\left[1 - \frac{(f - f_{\text{ULCO}})}{(f_{\text{Pmin}} - f_{\text{ULCO}})}\right]$$		P
	The inverter power output level shall remain at or below the lowest power output level reached in response to the increase in frequency between f_{ULCO} and f_{Pmin}. This is to provide hysteresis in the control of the inverter. When the frequency has decreased below ($f_{ULCO} - f_{hyst}$), for at least 20 s, the inverter shall return to continuous operation. Any change in power output level shall be at a rate no greater than the power rate limit (W_{Gra}) of Clause 3.3.4. As shown in Figure 4.3.	See test data	P
4.5.3.3.2	Response to an increase in frequency for multiple mode inverters with energy storage		P

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Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	The response to an increase in frequency for multiple mode inverters with energy storage is a two-stage response. The initial stage is a reduction in the power output level if the inverter is generating, the second stage requires the inverter to increase its power input level through the grid-interactive port as the frequency continues to increase.		P
	When a disturbance results in an increase in frequency that exceeds the continuous operation range of (f_{ULCO}), the multiple mode inverter that is charging the energy storage via the grid-interactive port shall maintain at least the same power input level with the increase in frequency until ftransition is reached.		P
	When a disturbance results in an increase in frequency that exceeds the continuous operation range of (f_{ULCO}), the multiple mode inverter that is generating (from any energy source) shall reduce the power output linearly with the increase in frequency until $f_{transition}$ is reached. The power output level present at the time the frequency exceeds f_{ULCO} shall be held as the reference power output level used to calculate the required response to the increase in frequency.		P
	When a disturbance results in an increase in frequency that exceeds $f_{transition}$, the multiple mode inverter shall increase the power input level through the grid-interactive port, linearly with the increase in frequency until f_{Pmin} is reached, the maximum charge rate of the energy storage is reached, or the state of charge of the energy storage is full.		P
	The inverter power output level shall remain —		P
	(a) at or below the lowest power output level reached in response to the increase in-frequency between fULCO and ftransition; or		P
	(b) at or above the highest power input level reached in response to the increase in frequency between ftransition and fPmin (unless the state of charge of the energy storage is full).		P
	This is to provide hysteresis in the control of the inverter. When the frequency has decreased below (fULCO − fhyst), for at least 20 s, the power level of the inverter shall be restored to the pre-disturbance level at a rate no greater than the power rate limit (WGra) of Clause 3.3.4.		P
4.5.4	Voltage disturbance withstand		P
4.5.4.1	General		P
	A voltage disturbance is any variation of voltages outside of the voltage limits continuous operation of Table 4.8. The inverter or inverter energy system shall respond as specified in Table 4.8 for voltage disturbances.	See test data	P
	The inverter shall cease power generation within 200 ms after the measured voltage falls below or exceeds the continuous operation limits. For voltage disturbances lasting less than the trip delay times in Table 4.1, the inverter shall restore active power output to the pre-disturbance level within 400 ms after the measured voltage has returned to within the continuous operation limits of Table 4.8.		P

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Clause	Requirement – Test	Result - Remark	Verdict

	For a three-phase inverter, the inverter shall respond in the event of a voltage disturbance on any of the phases.	Not three-phase inverter	N/A
	For a multiple mode inverter meeting the performance classification for output requirements of AS IEC 62040.3 that provides an operational mode to supply load continuously during grid disruption, the inverter may disconnect the grid-interactive port in place of the cease power generation requirement, provided that when the grid voltage recovers within the voltage requirements of the AS IEC 62040.3 performance classification relevant to the inverter, the inverter shall restore active power output through the grid-interactive port to the pre-disturbance level within 400 ms.		P
	Compliance shall be determined by type testing in accordance with the voltage disturbance withstand test specified in Appendix I.	See test data	P
4.5.4.2	Multiple voltage disturbances		P
	A multiple voltage disturbance event is any number of voltage disturbances as defined in Clause 4.5.4.1 where the cumulative time that the voltage is less than the trip delay time as specified in Table 4.1, provided that each voltage disturbance occurs no more than 15 s since the previous disturbance. After a period of 15 s without a disturbance, any further disturbances shall be treated as a new multiple voltage disturbance event. Refer to Figure 4.5 for example of a multiple voltage disturbance event.		P
	The inverter shall respond in accordance with the requirements of Clause 4.5.4.1 in the event of multiple voltage disturbances. The inverter shall not disconnect for at least two multiple voltage disturbance events. The inverter may disconnect in the event of any further voltage disturbance within the following 20 minute period.		P
	Compliance shall be determined by type testing in accordance with the multiple voltage disturbance withstand test specified in Appendix I.	See test data	P
4.5.5	Voltage phase angle shift withstand		P
	The inverter shall remain in continuous operation for a single-phase voltage angle shift within a voltage cycle of at least 60 electrical degrees. In addition, three-phase inverters shall remain in continuous operation for a voltage phase angle shift within a voltage cycle, in the positive-sequence, of at least 20 electrical degrees. Refer to Table 4.9.		P
	Compliance shall be determined by type testing in accordance with the voltage phase angle shift withstand test specified in Appendix I.	See test data	P
4.5.6	Rate of change of frequency		P
	The inverter shall maintain continuous operation for frequency excursions with a rate of change of frequency (ROCOF) that do not exceed ± 4.0 Hz/s for a duration of 0.25 s.		P
	Compliance shall be determined by type testing in accordance with the sustained operation for frequency variations test specified in Appendix J.	See test data	P
4.6	Disconnection on external signal		P

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Clause	Requirement – Test	Result - Remark	Verdict

Clause	Requirement – Test	Result - Remark	Verdict
	The automatic disconnection device shall incorporate the ability to disconnect on an external signal.		P
	If an external signal or demand response "DRM 0" condition is asserted, the automatic disconnection device shall operate within 2 s.		P
	Compliance shall be determined by type testing as specified in Appendix E.	See test data	P
4.7	Connection and reconnection procedure		P
	Only after all of the following conditions have been met shall the automatic disconnection device operate to connect or reconnect the inverter to the grid —		P
	(a) the voltage has been maintained within the utilization limits of AS 60038 (for Australia) or the utilization limits (for New Zealand) for at least 60 s;		P
	(b) the frequency has been maintained within the range 47.5 Hz to 50.15 Hz for at least 60 s;		P
	(c) the inverter and the grid are synchronized and in-phase with each other; and		P
	(d) no external signal is present or DRM 0 asserted requiring the system to be disconnected.		P
	After the automatic disconnection device operates to connect or reconnect the inverter the output shall rate limit increase in power generation to the set power rate limit (WGra) for increase in power of Clause 3.3.4. Unconstrained power operation may recommence after the automatic disconnection device operates to connect or reconnect the inverter, when either the rated power output is reached or the required power output level of the inverter exceeds the available energy source.		P
	Compliance shall be determined by type testing in accordance with the tests as specified in Appendix H and Appendix I.	See test data	P
4.8	Security of protection settings		P
	The settings of the automatic disconnection device shall be secured against inadvertent or unauthorized changes. Changes to the settings shall require the use of a tool and special instructions not provided to unauthorized personnel.	Considered	P
	The settings, specified in Clause 4.5, shall only be capable of being adjusted within the limits specified in Clause 4.5.		P
	The limit values of the automatic disconnection device, specified in Clause 4.4, shall be secured against changes.		P
	The specific regional settings selected for Australia or New Zealand, once applied or confirmed for each inverter, shall be secured against unauthorized changes. NOTE Special interface devices and passwords are regarded as tools.		P
	Compliance shall be determined by inspection.		P
4.9	Activation of protection settings		P
	The inverter shall not operate the automatic disconnection device to connect until a regional setting has been selected and activated by an authorized person.	See test data	P
	Variations to default regional configuration settings of this Section (4) shall be within the ranges specified within this Section (4).		P

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Clause	Requirement – Test	Result - Remark	Verdict
	Where the inverter does not connect due to no selection or activation of a regional configuration, the inverter shall provide a visible alert.		P
	The inverter settings shall be able to be viewed in read-only mode for verification. A set of operational instructions for viewing inverter regional setting shall be available. Inverter regional settings may be displayed via a panel/screen, external device or software interface.		P
5	Multiple inverter combinations		N/A
5.1	General		N/A
	There are installations where multiple inverter energy systems are used and the electrical installation connects at a single point of supply to the grid. Inverter energy systems are often comprised of multiple inverters used in combination to provide the desired inverter energy system capacity or to ensure that voltage balance is maintained in multiple-phase connections to the grid.		N/A
	This Section (5) specifies the requirements and tests for inverter energy systems used in such combinations. If a combination is not tested, it should not be used or external devices should be used in accordance with the requirements of AS/NZS 4777.1.		N/A
	Possible combinations are single-phase inverters used in parallel, single-phase inverters used in multiple-phase installations and three-phase inverters used in parallel.		N/A
5.2	Inverter current balance across multiple phases		N/A
	In a multiple-phase inverter energy system comprised of individual single-phase inverters, the a.c. current output should be generated and injected into the multiple-phase electrical installation to minimize current imbalance. The maximum current imbalance in a multiple-phase inverter energy system comprised of either individual single-phase inverters connected on separate phases or a combination of single-phase inverters and multiple-phase inverters shall not exceed 21.7 A for more than 15 s. NOTE 1 This maximum current imbalance also applies to multiple mode inverters used in a inverter energy system that may have a charging mode. NOTE 2 Provisions for current balance of three-phase inverters are given in Clause 2.11.		N/A
5.3	Grid disconnection		N/A
	When any inverter (single-phase or multiple-phase) within a multiple-phase inverter energy system disconnects as required by Section 4, all inverters within the multiple-phase inverter energy system shall disconnect within 2 s of the first inverter disconnecting. This applies to all inverters used in combination for multiple phases.		N/A
5.4	Grid connection and reconnection		N/A
	When multiple inverters are used together in a multiple-phase combination, only after all the conditions of Clause 4.7 have been met on all connected phases shall the automatic disconnection device operate to connect or reconnect any inverter of the multiple-phase combination to the grid.		N/A

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Clause	Requirement – Test	Result - Remark	Verdict
	Where any inverter used in a multiple-phase combination has a rated current exceeding 21.7 A per phase, the requirement of Clause 5.2 shall be met when connecting or reconnecting.		N/A
5.5	Testing combinations		N/A
5.5.1	Single-phase combinations		N/A
	Single-phase parallel combinations of inverters shall be tested for combinations with total rated current (Irated) equal to or up to the maximum of 6 A per phase.		N/A
	To determine the number of inverters to be tested, the following equation shall be used: $$N = \frac{6}{I_{\text{rated}}}$$		N/A
	If N ≥ 2, the minimum number of inverters to be tested shall be N. If N > 6, the maximum number of inverters to be tested in a combination shall be 6.		N/A
5.5.2	Single-phase inverters used in three-phase combinations		N/A
	For single-phase inverters with rated current (Irated) greater than or equal to 5 A used in three-phase combinations, three inverters shall be tested in a three-phase arrangement [refer to Figure 5.1(a)].		N/A
	Single-phase inverters with rated current less than 5 A and to be used in three-phase combinations shall be tested in combination with at least two inverters per phase [refer to Figure 5.1(b)]. NOTE Testing of combinations is not required if the test combination is not allowed by the inverter manufacturer's installation instructions or similar documentation.		N/A
5.5.3	Required tests for multiple inverter combinations		N/A
	Any single-phase inverter used in a multiple inverter combination shall be tested individually and meet all the requirements of this Standard. Any single-phase inverter that is to be used as part of a multiple inverter combination shall be tested in combination as specified in Clauses 5.5.1 and 5.5.2.		N/A
	The tests specified in Table 5.1 for multiple inverter combinations shall be performed.		N/A
5.5.4	Multiple inverters with one automatic disconnection device		N/A
	Where the inverter does not have an internal automatic disconnection device, or requires an external automatic disconnection device to provide the required disconnection function, or both, testing shall be conducted with the automatic disconnection device and with either the number of inverters required by Clause 5.5.1 and 5.5.2 or with the automatic disconnection device configured with the number of inverters specified by the manufacturer's instructions.		N/A
	Compliance shall be determined by performing all of the type tests specified in Clause 5.5.		N/A
6	Generation control function		P
6.1	General		P

AS/NZS 4777.2		
Clause	Requirement – Test	Result - Remark	Verdict
	The generation control function is used to control the active or apparent power output levels of an inverter or multiple inverter combination such that it meets a predetermined generation output level that may be less than the total rated apparent power of the inverter or multiple inverter combination. Two generation control functions should be provided as inverter functions, these are —		P
	(a) generation limit control; and		P
	(b) export limit control.		P
	This Section (6) applies to an inverter or multiple inverter combinations that have either or both generation control functions. Where included in the inverter, these generation control functions shall be disabled by default.		P
	The generation control function for an inverter or multiple inverter combination should operate with the following limits:		P
	(i) Soft limit: A limit that will cause the inverter or multiple inverter combination to reduce its output, preventing generation greater than the limit.		P
	(ii) Hard limit: A limit that when activated will cause the inverter or multiple inverter combination to disconnect (e.g. when the soft limit has not been met).		P
	The soft limit may be utilized with the hard limit to minimize the number of disconnections due to exceeding the hard limit. Where both hard and soft limits are used the requirements for hard limit shall take precedence over the soft limit requirements.		P
	The generation control function shall monitor the response of the inverter or multiple inverter combination to the soft limit and hard limit. Where a fault or loss of operability is detected the generation control function shall respond such that on failure of —		P
	(A) the soft limit function, reduce the output of the inverter or multiple inverter combination to zero within 15 s; and		P
	(B) the hard limit function, operate the automatic disconnection device within 5 s.		P
	For multiple-phase systems, the generation control functions shall monitor and control the generation on each phase.		N/A
	The generation control may use inverter internal measurements or external sensors for measurements. All measurement for generation control functions shall conform to Table 2.5 specifications. The generation control function may be integrated into the inverter or use an external controller. NOTE The external controller may be another inverter in the multiple inverter combination.		P
	Where an external measurement device or controller is used, any loss of signal or failure of the device shall cause the inverter or multiple inverter combination to operate the automatic disconnection device and disconnect within 5 s, unless the only generation limit control activated is a soft export limit, in which case the inverter or multiple inverter combination shall reduce active power output to the soft export limit setting as a maximum within 15 s.	External measurement device: manufacturer Afore, model SAPM-10KW	P

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Clause	Requirement – Test	Result - Remark	Verdict
	The connection to external devices shall be re-established and achieve stable operation for at least 15 s before the inverter or multiple inverter combination reconnects in accordance with Clause 4.7.		P
	Compliance shall be determined by type testing in accordance with the generation control function test specified in Appendix L.	See test data	P
6.2	Generation limit control		P
6.2.1	General		P
	The generation limit control function provides control of the apparent power output level of an inverter or multiple inverter combination within an electrical installation. The generation limit control function may be integrated into the inverter or an external device.		P
	The generation limit control for an inverter or multiple inverter combination shall limit the apparent power output level, specified as an apparent power value (VA). The generation limit control function shall have a hard limit and a soft limit specified, where the soft limit coordinates with the hard limit.		P
	Where a generation limit has been applied the generation limit shall be substituted for the inverter or multiple inverter combination rated apparent power for determining the corresponding level of response for the power quality response modes of the inverter or multiple inverter combination. For multiple inverter combinations, including multiple-phase systems, the generation limit shall apply to the net apparent power output at the point of generation.		P
	In multiple-phase systems the apparent power level shall be balanced across the phases.		P
6.2.2	Soft limit		P
	For the generation limit control function a soft limit shall be utilized to control the apparent power output level such that the hard limit is not exceeded.		P
	Where the soft limit is exceeded, the generation limit control function shall operate to reduce the apparent power output of the inverter or multiple inverter combination to less than the soft limit within 15 s.		P
6.2.3	Hard limit		P
	Where the hard limit is exceeded for 15 s the generation limit control function shall operate to disconnect the inverter or each inverter within the multiple inverter combination within 5 s.		P
6.3	Export limit control		P
6.3.1	General		P
	The export limit control function for an inverter is used to control the generation from an inverter or multiple inverter combination to manage the export power level from an electrical installation to the grid. The export limit control function may be integrated into the inverter or an external device.		P

AS/NZS 4777.2		
Clause	Requirement – Test	Result - Remark	Verdict
	The export limit control for an inverter or multiple inverter combination shall limit the active power export level, specified as an active power value (W). The export limit may be set to allow export to the grid or to provide a minimum import load from the grid.		P
	For inverter or multiple inverter combinations, including multiple-phase systems, the export limit shall apply to the net active power level at the point of supply across all phases.		P
6.3.2	Soft limit		P
	For the export limit control function, where the soft limit is exceeded the export limit control function shall operate to reduce the power output of the inverter or multiple inverter combination such that the export limit of the electrical installation is met within 15 s.		P
6.3.3	Hard limit		P
	For inverter or multiple inverter combination the hard limit may be applied. For the export limit control function, where the hard limit is exceeded the export limit control function shall operate to disconnect the inverter or each inverter within the multiple inverter combination within 5 s.		P
7	Inverter marking and documentation		P
7.1	General		P
	The inverter shall conform to the marking and documentation requirements of IEC 62109-1 and IEC 62109-2, as varied by this Section (7).		P
	All markings and documentation shall be in the English language. NOTE The marking and documentation may be written in other languages in addition to English.		P
7.2	Marking		P
7.2.1	General		P
	The following variations apply to the marking requirements of IEC 62109-1 and IEC 62109-2:		P
	(a) Inverters that are designated for use in inverter energy systems incorporating energy sources other than PV arrays or batteries shall bear additional or alternative markings applicable to the energy source.		P
	(b) Inverters that are designated for use in closed electrical operating areas shall be marked with a warning stating that they are not suitable for installation in households or areas of a similar type or use (i.e. domestic). NOTE This requirement is derived from the Cooling system failure—Blanketing test of IEC 62109-2. It is intended to ensure that inverters for closed electrical operating areas are not installed in areas where the intended ventilation may be blocked after installation due to shared access and use. For example, an inverter may be installed with correct ventilation in a storage area, but over time the area may become cluttered with material that blocks required ventilation and rests against the heat sink, preventing adequate cooling of the device.		P
7.2.2	Equipment ratings		P

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Clause	Requirement – Test	Result - Remark	Verdict
	The inverter shall be marked with its ratings and the ratings of each port, as specified in Table 7.1. Only those ratings that are applicable to the type of inverter are required. The ratings shall be plainly and permanently marked on the inverter, in a location that is clearly visible after installation.		P
7.2.3	Ports		P
	Each port shall be marked with its classification and indicate whether a.c. or d.c. voltage as applicable.		P
	Typical classifications for input, output and communication ports include the following:		P
	a) PV (photovoltaic). (b) Wind turbine. (c) Energy storage. (d) Battery. (e) Generator. (f) Grid-interactive. (g) Stand-alone. (h) a.c. input. (i) Load. (j) Communications (type). (k) DRM.		P
7.2.4	External and ancillary equipment		P
	If the inverter requires external or ancillary equipment for compliance with this Standard, the requirement for any such equipment shall be marked on the inverter along with the following or an equivalent statement: Refer to the installation instructions for type and ratings or symbol. NOTE External or ancillary equipment includes external automatic disconnection devices, external isolation transformers and external RCDs.	See waring marking. The external meter for generation control shall be installed.	P
	Any external or ancillary equipment shall be marked in accordance with this Section (7).		P
7.2.5	Residual current devices (RCDs)		P
	Inverter energy systems used with PV array systems require residual current detection in accordance with IEC 62109-1 and IEC 62109-2. The requirements can be met by the installation of a suitably rated RCD external to the inverter or by an RCMU integral to the inverter.	Integrated RCMU used for residual current detection in accordance with IEC 62109-1 and IEC 62109-2.	P
	Where an external RCD is required, the inverter shall be marked with a warning along with the rating and type of RCD required. The warning shall be located in a prominent position and written in lettering at least 5 mm high. It shall contain the following or an equivalent statement: **WARNING — AN RCD IS REQUIRED ON THE [NAME] PORTS OF THE INVERTER**		N/A
	If the inverter energy system requires a type B RCD, the inverter shall be marked with a warning. The warning shall be located in a prominent position and written in lettering at least 5 mm high. It shall contain the following: **WARNING — A TYPE B RCD IS REQUIRED ON THE [NAME] PORTS OF THE INVERTER**		N/A
7.2.6	Demand response modes		P

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Clause	Requirement – Test	Result - Remark	Verdict
	The demand response modes supported by the inverter should be permanently marked on the name plate or on a durable sticker to indicate the demand response modes of which the unit is capable. Where the inverter utilizes a demand response interface port an alternative location for the marking where not on nameplate should be on or near that port.		P
	Figure 7.1 illustrates a permitted form of marking. If this form of marking is used, each box shall contain a tick or a cross (if the inverter has that capability) or remain blank (if it does not have that capability). Alternatively, only the modes supported may be marked.		P
	If the physical interface is a terminal block, then —		P
	(a) the terminals shall be engraved or otherwise durably marked; or		P
	(b) a permanent label with "DRM Port" shall be affixed near the terminal block.		N/A
	The marking shall indicate which terminal corresponds to which demand response mode. The range of markings is indicated against Pins 1 to 6 in Table 3.4.		N/A
	The following contractions are permitted:		N/A
	(i) "DRM" may be omitted, e.g. the terminal corresponding to DRM 1 may be marked "1" and the terminal corresponding to DRM 1/5 may be marked "1/5".		N/A
	(ii) "Common" may be contracted to "C".		N/A
	(iii) "RefGen" may be contracted to "Gen".		N/A
	(iv) "Com/DRM 0" may be contracted to "CD0".		N/A
7.3	Documentation		P
7.3.1	General		P
	The documentation supplied with the inverter shall provide all information necessary for the correct and safe installation, operation, maintenance and use of the system and any required external devices including information specified in Clause 7.2.		P
	All inverters, including those intended for use in systems incorporating energy sources other than PV arrays or batteries, shall conform to the documentation requirements of IEC 62109-1 and IEC 62109-2.		P
	Inverter documentation shall include a description of the type of inverter as either a grid-interactive or stand-alone inverter, in accordance with the requirements of this Standard. There may be additional descriptions related to the energy source/s or whether it also is a multiple mode inverter with various other modes of operation.		P
	Inverter documentation shall include specification of environmental condition that it is intended for and the rated maximum operating ambient temperature that shall not be less than —		P
	(a) 40 °C for indoor conditioned;		N/A
	(b) 50 °C for indoor unconditioned;		N/A
	(c) 50 °C for outdoor unconditioned without solar effects; or		N/A

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Clause	Requirement – Test	Result - Remark	Verdict
	(d) 60 °C for outdoor unconditioned with solar effects. NOTE Without solar effects means that the inverter is installed in a location not subject to solar radiation as per AS 60947.3.		P
7.3.2	Equipment ratings		P
	The documentation supplied with the inverter shall state the ratings of the inverter and the ratings for each port and parameter listed in Table 7.2. Only those ratings that are applicable to the type of inverter are required.		P
	For equipment with rated current greater than 16 A per phase, additional documentation requirements apply. See Clause 2.8.		P
7.3.3	Ports		P
	In addition to the requirements of Clause 7.3.2, the documentation supplied with the inverter shall state the following for each port, as a minimum:		P
	(a) Means of connection.	See instruction manual	P
	(b) For pluggable equipment type B, the type of matching connectors to be used. NOTE 1 For some ports, the specific manufacturer of the connector type may also need to be specified to ensure correct mating connectors.		N/A
	(c) External controls and protection requirements.	See instruction manual	P
	(d) Explanation of terminals or pins used for connection including polarity and voltage.	See instruction manual	P
	(e) Tightening torque to be applied to terminals.	See instruction manual	P
	(f) Instructions for protective earthing.	See instruction manual	P
	(g) Instructions for connection of loads and installation of RCD protection to stand-alone ports.	See instruction manual	P
	(h) The decisive voltage class (DVC). NOTE 2 The DVC is the voltage of a circuit which occurs continuously between any two live parts in the worst-case rated operating condition when used as intended.	See instruction manual	P
	In addition to port documentation, where the port has an isolating device as part of and within the inverter as described in Clause 2.12 the following ratings are required —	See instruction manual	P
	(i) rated insulation voltage;	See instruction manual	P
	(ii) rated impulse withstand voltage;	See instruction manual	P
	(iii) suitability for isolation;	See instruction manual	P
	(iv) rated operational current;	See instruction manual	P
	(v) utilization category and/or PV utilization category;	See instruction manual	P
	(vi) rated short-time withstand current (Icw);	See instruction manual	P
	(vii) rated short-circuit making capacity (Icm); and	See instruction manual	P
	(viii) rated breaking capacity. NOTE 3 The definitions for Icw and Icm are the same as used in AS 60947.3.	No switching device	N/A
7.3.4	External and ancillary equipment		P
	Where an inverter or multiple inverter combinations requires external or ancillary equipment to achieve functional requirements of this Standard, the documentation shall —		P

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Clause	Requirement – Test	Result - Remark	Verdict

	(a) state the requirement for any such equipment;	The external meter for generation shall be installed.	P
	(b) provide sufficient information to identify the external or ancillary equipment, either by manufacturer and part number or by type and rating; and	See instruction manual	P
	(c) specify assembly, location, mounting and connection requirements.	See instruction manual	P
7.3.5	Residual current devices (RCDs)		P
	Where an external RCD is required, the following or an equivalent statement shall be included in the documentation: "External RCD required". The documentation shall also state the rating and type of RCD required and provide instructions for the installation of the RCD.	See instruction manual	P
7.3.6	Multiple mode inverters		P
	Where the inverter is capable of multiple mode operation, the documentation shall include the following:		P
	(a) Ratings and means of connection to each source of supply to the inverter or output from the inverter.	See instruction manual	P
	(b) Any requirements related to wiring and external controls, including the method of maintaining neutral continuity within the electrical installation to any stand-alone ports as required.	See instruction manual	P
	(c) Disconnection means and isolation means.	See instruction manual	P
	(d) Overcurrent protection needed.	See instruction manual	P
7.3.7	Multiple inverter combinations		N/A
	Where an inverter has been tested for use in a multiple inverter combination as per Section 5, the documentation shall include the following:		N/A
	(a) Valid combinations of inverters.		N/A
	(b) Installation instructions for correct operation as a multiple inverter combination.		N/A
7.3.8	Firmware		P
	The documentation shall provide instructions for viewing of the inverter firmware version and the selected regional settings and any variations to the default inverter settings in read-only mode. This is to prevent unauthorized modification of inverter settings.		P
	Documentation on the initial configuration and selection of regional settings and other settings at commissioning shall be provided to authorized persons.		P
	Restricted information on accessing and changing the regional settings, other settings and firmware after initial configuration shall be provided to authorized persons only.		P
Appendix A	General test and reporting requirements	See test data	P
Appendix B	Harmonic current limit test	See test data	P
Appendix C	Transient voltage limit test	See test data	P

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Clause	Requirement – Test	Result - Remark	Verdict
Appendix D	DC injection test	See test data	P
Appendix E	Demand response mode testing including disconnection on external signal	See test data	P
Appendix F	Fixed power factor mode and reactive power mode test	See test data	P
Appendix G	Power quality (voltage) response mode testing	See test data	P
Appendix H	Active anti-islanding test	See test data	P
Appendix I	Voltage and frequency limits tests	See test data	P
Appendix J	Sustained operation test procedures	See test data	P
Appendix K	Multiple inverter testing		N/A
Appendix L	Generation control function testing	See test data	P
Appendix M	Stand-alone inverters		N/A

Attachment 1 Photos

Overview-AF6K-SL
Overview-AF6K-SL

Appendix1 Photos:

Overview-AF6K-SL
Overview-AF6K-SL

Appendix1 Photos:

Overview-AF6K-SL
Overview-AF6K-SL

Appendix1 Photos:

Internal view-AF6K-SL
Internal view-
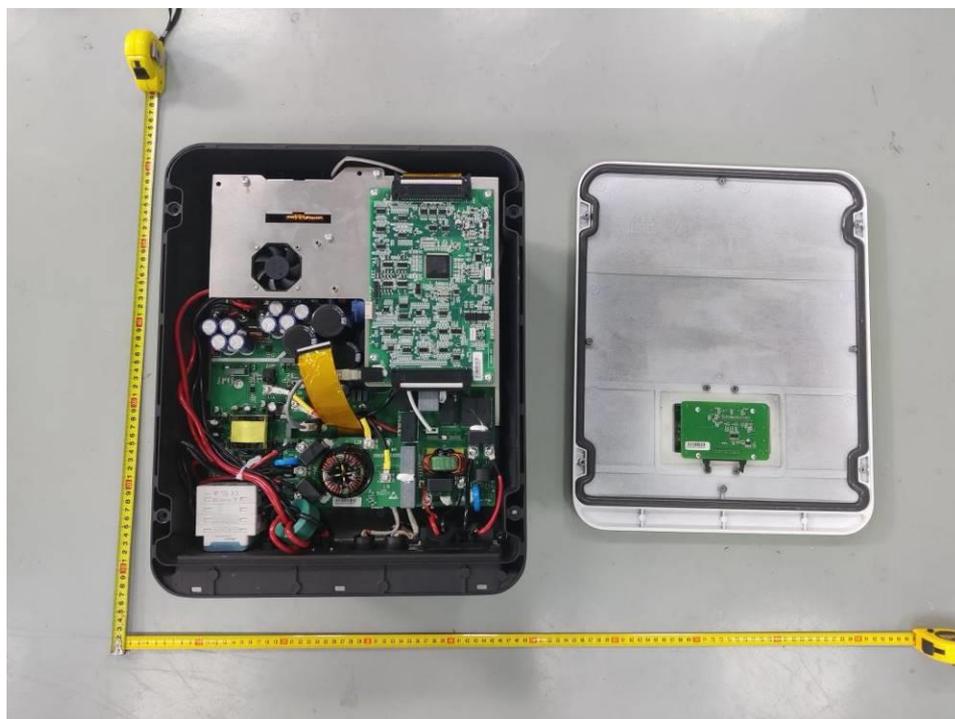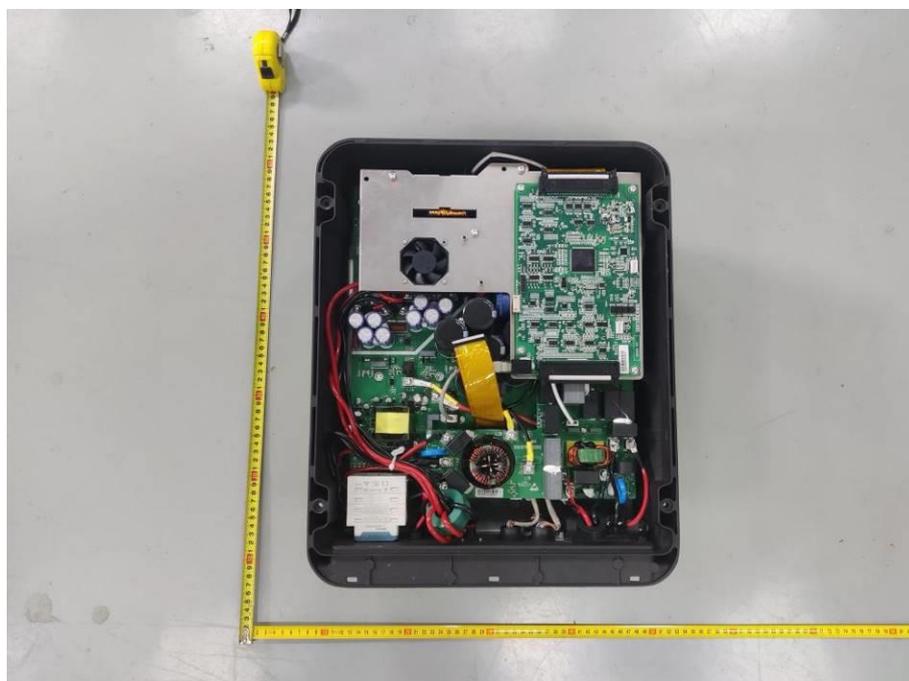
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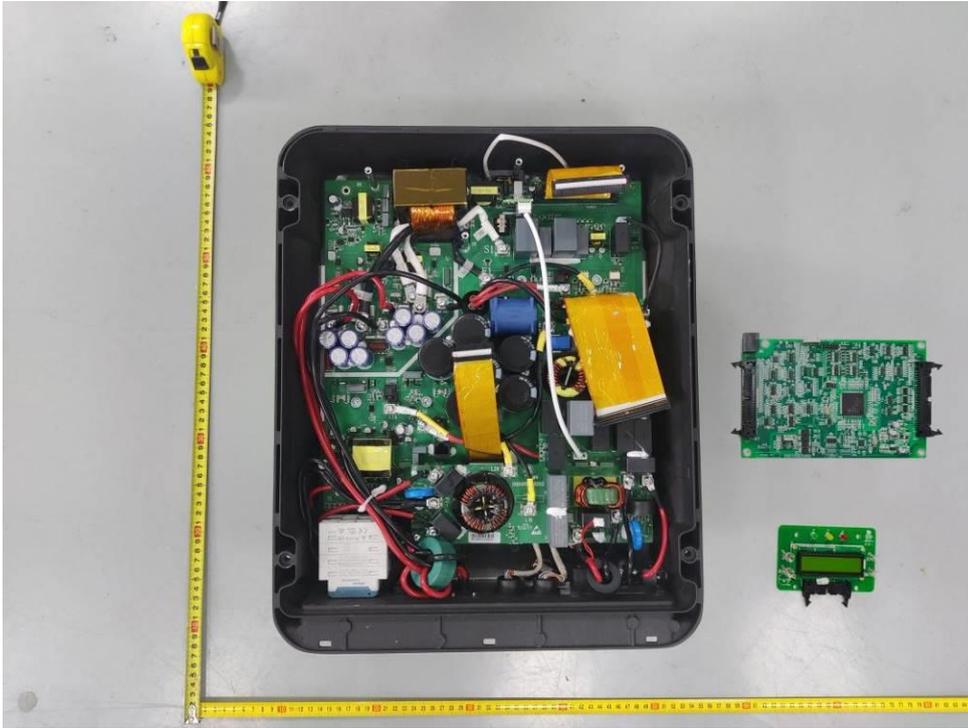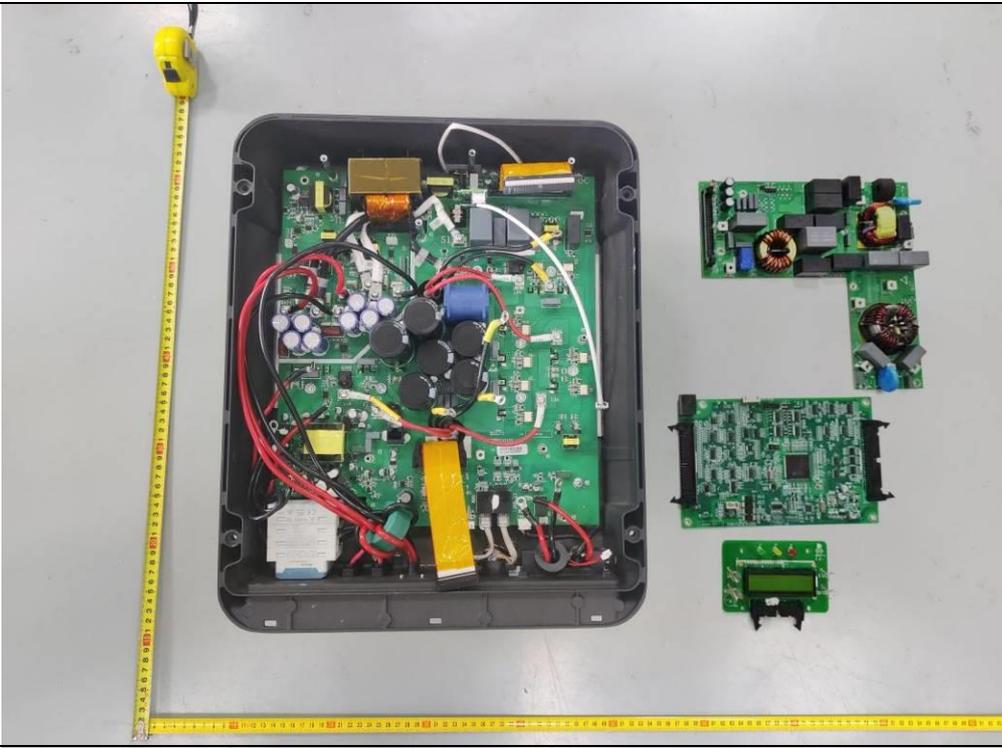
Internal view-
Internal view-

Appendix1 Photos:

Internal view-
Internal view-

Appendix1 Photos:

Internal view-
Internal view-

Appendix1 Photos:

Internal view-
Internal view-

Appendix1 Photos:

Password input
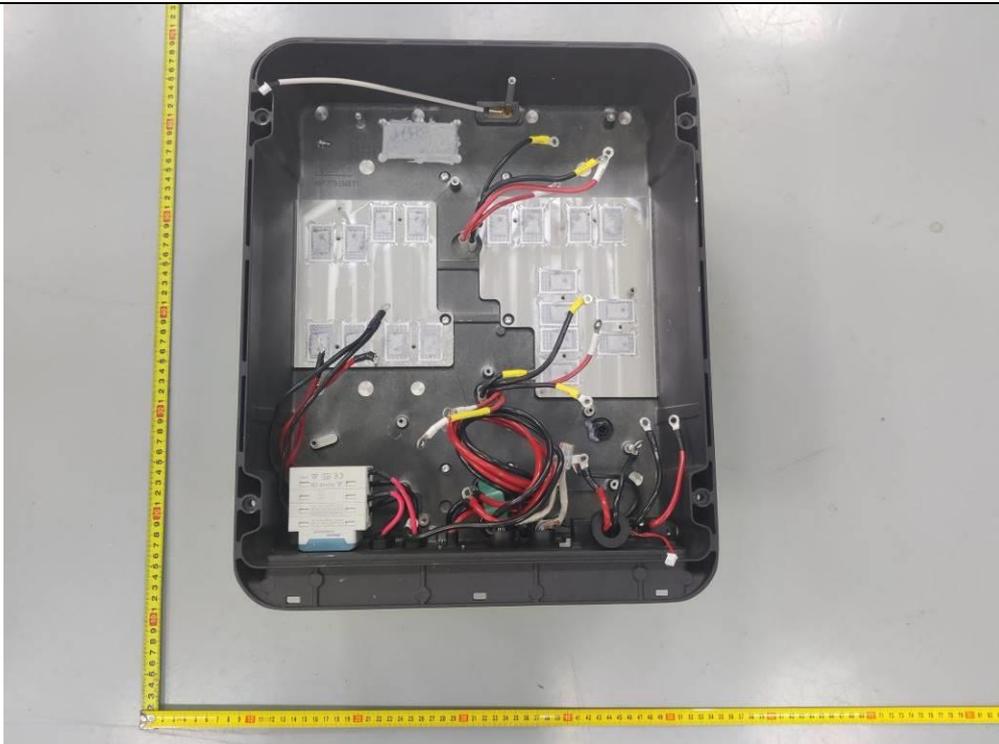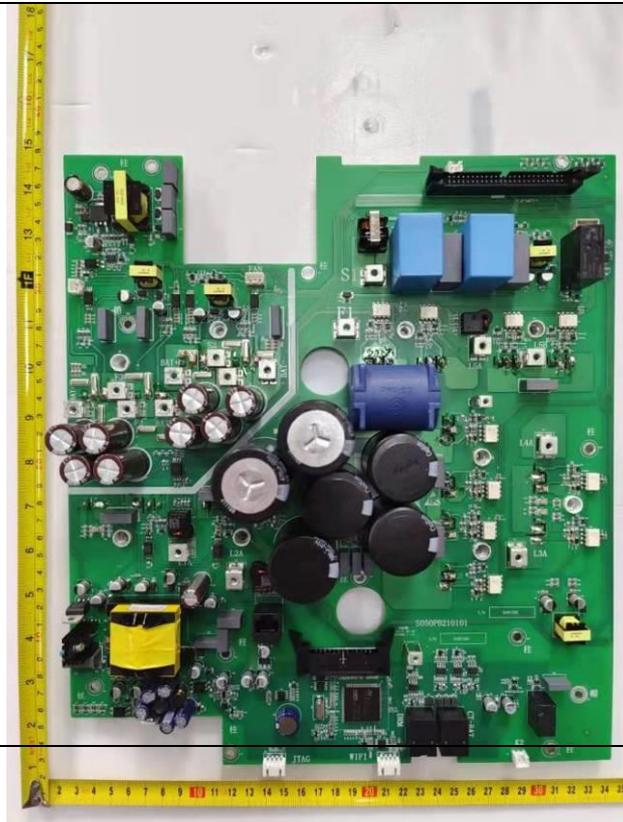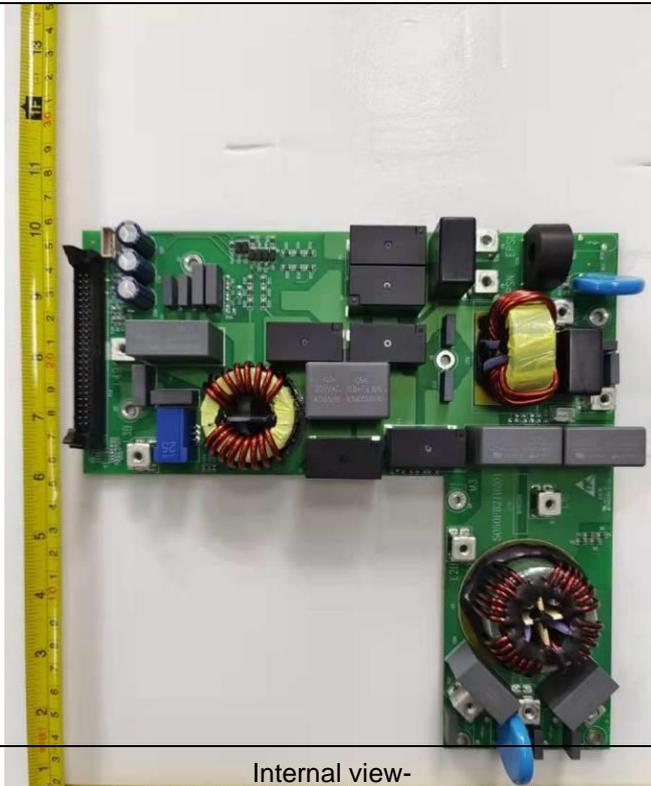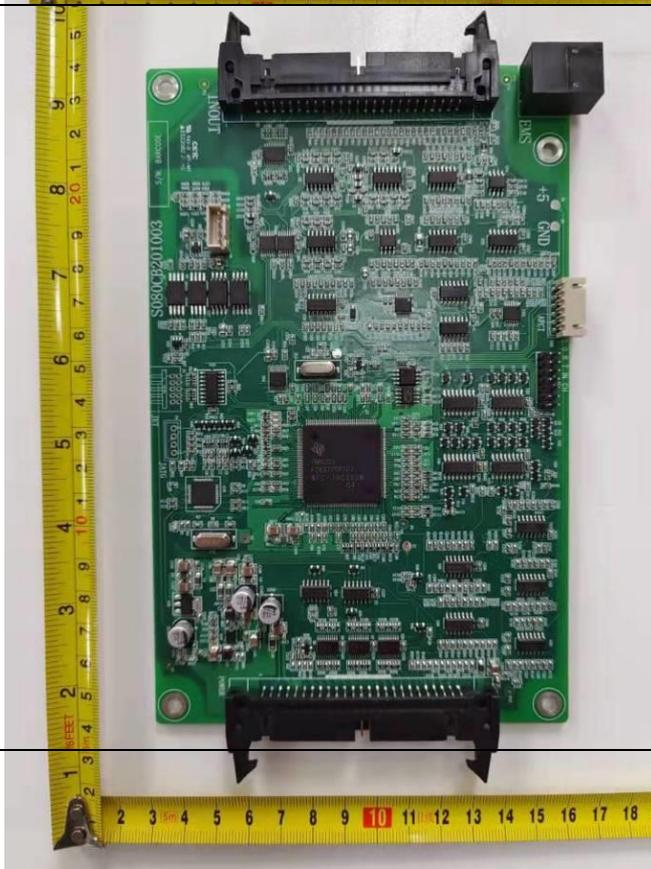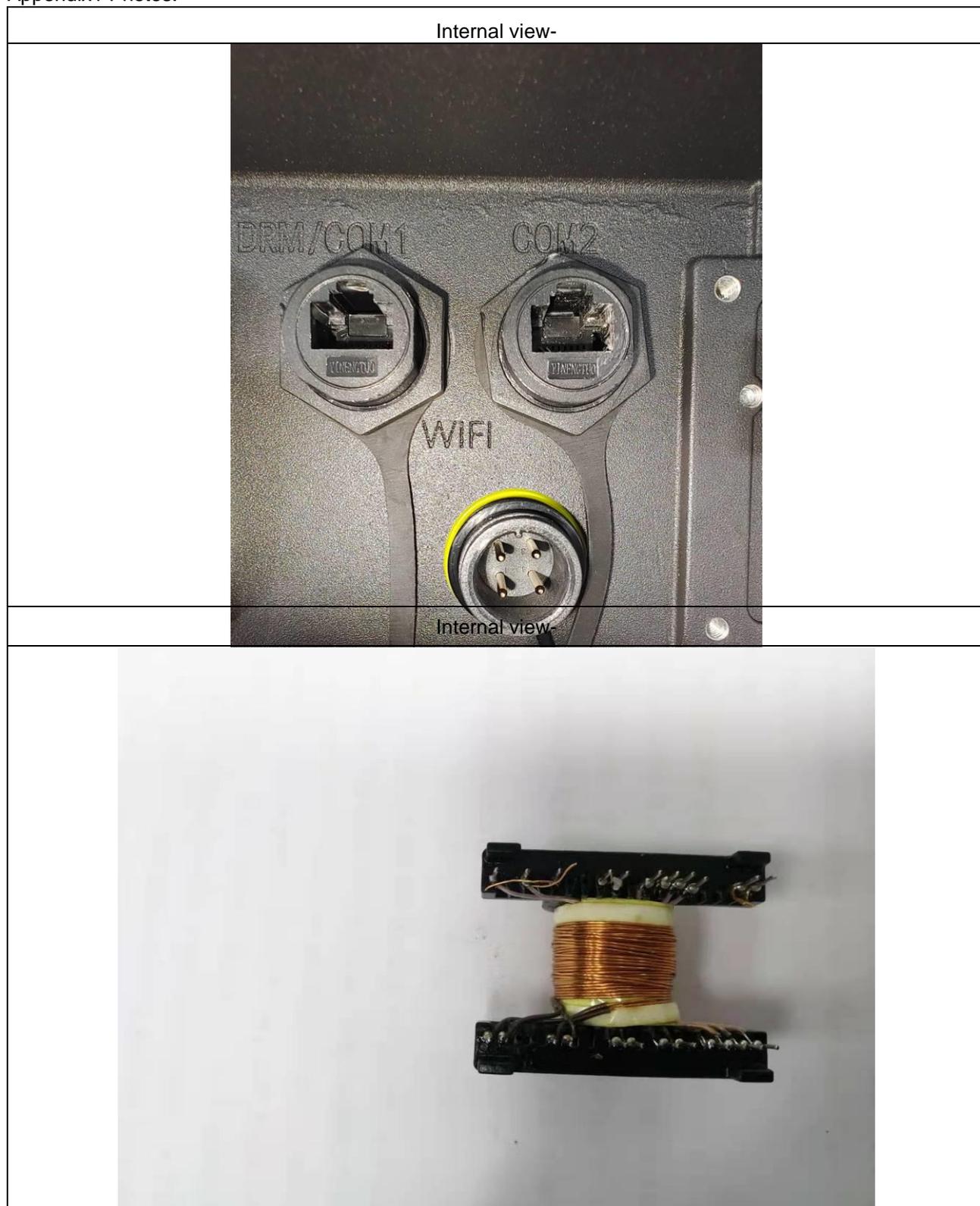
Attachment 2 Test Data

3.4.2	Sinusoidal output in stand-alone mode- 5%Pn						P
Model: AF6K-SL							
Harmonic	Value V			$U_{harmonic}$ of fundamental			Limit in % of fundamental
	L1 Phase	L2 Phase	L3 Phase	L1 Phase	L2 Phase	L3 Phase	
2nd	0.244	N/A	N/A	0.106%	N/A	N/A	5%
3rd	2.887	N/A	N/A	1.255%	N/A	N/A	5%
4th	0.090	N/A	N/A	0.039%	N/A	N/A	5%
5th	0.246	N/A	N/A	0.107%	N/A	N/A	5%
6th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
7th	1.382	N/A	N/A	0.601%	N/A	N/A	5%
8th	0.182	N/A	N/A	0.079%	N/A	N/A	5%
9th	1.194	N/A	N/A	0.519%	N/A	N/A	5%
10th	0.120	N/A	N/A	0.052%	N/A	N/A	5%
11th	0.311	N/A	N/A	0.135%	N/A	N/A	5%
12th	0.092	N/A	N/A	0.040%	N/A	N/A	5%
13th	0.662	N/A	N/A	0.288%	N/A	N/A	5%
14th	0.166	N/A	N/A	0.072%	N/A	N/A	5%
15th	0.706	N/A	N/A	0.307%	N/A	N/A	5%
16th	0.145	N/A	N/A	0.063%	N/A	N/A	5%
17th	0.393	N/A	N/A	0.171%	N/A	N/A	5%
18th	0.092	N/A	N/A	0.040%	N/A	N/A	5%
19th	0.465	N/A	N/A	0.202%	N/A	N/A	5%
20th	0.156	N/A	N/A	0.068%	N/A	N/A	5%
21th	0.469	N/A	N/A	0.204%	N/A	N/A	5%
22th	0.133	N/A	N/A	0.058%	N/A	N/A	5%
23th	0.363	N/A	N/A	0.158%	N/A	N/A	5%
24th	0.127	N/A	N/A	0.055%	N/A	N/A	5%
25th	0.359	N/A	N/A	0.156%	N/A	N/A	5%
26th	0.145	N/A	N/A	0.063%	N/A	N/A	5%
27th	0.343	N/A	N/A	0.149%	N/A	N/A	5%
28th	0.122	N/A	N/A	0.053%	N/A	N/A	5%
29th	0.308	N/A	N/A	0.134%	N/A	N/A	5%
30th	0.138	N/A	N/A	0.060%	N/A	N/A	5%
31th	0.276	N/A	N/A	0.120%	N/A	N/A	5%
32th	0.143	N/A	N/A	0.062%	N/A	N/A	5%
33th	0.265	N/A	N/A	0.115%	N/A	N/A	5%
34th	0.117	N/A	N/A	0.051%	N/A	N/A	5%
35th	0.248	N/A	N/A	0.108%	N/A	N/A	5%
36th	0.131	N/A	N/A	0.057%	N/A	N/A	5%
37th	0.212	N/A	N/A	0.092%	N/A	N/A	5%
38th	0.131	N/A	N/A	0.057%	N/A	N/A	5%
39th	0.196	N/A	N/A	0.085%	N/A	N/A	5%
40th	0.108	N/A	N/A	0.047%	N/A	N/A	5%
41th	0.182	N/A	N/A	0.079%	N/A	N/A	5%
42th	0.110	N/A	N/A	0.048%	N/A	N/A	5%

43th	0.147	N/A	N/A	0.064%	N/A	N/A	5%
44th	0.108	N/A	N/A	0.047%	N/A	N/A	5%
45th	0.131	N/A	N/A	0.057%	N/A	N/A	5%
46th	0.087	N/A	N/A	0.038%	N/A	N/A	5%
47th	0.124	N/A	N/A	0.054%	N/A	N/A	5%
48th	0.083	N/A	N/A	0.036%	N/A	N/A	5%
49th	0.106	N/A	N/A	0.046%	N/A	N/A	5%
50th	0.081	N/A	N/A	0.035%	N/A	N/A	5%
THD	N/A	N/A	N/A	1.760%	N/A	N/A	5%

3.4.2	Sinusoidal output in stand-alone mode- 50%Pn						P

Model: AF6K-SL

Harmonic	Uharmonic Value [V]			Uharmonic of fundamental			Limit in % of fundamental
	L1 Phase	L2 Phase	L3 Phase	L1 Phase	L2 Phase	L3 Phase	
2nd	1.902	N/A	N/A	0.827%	N/A	N/A	5%
3rd	3.071	N/A	N/A	1.335%	N/A	N/A	5%
4th	0.952	N/A	N/A	0.414%	N/A	N/A	5%
5th	2.369	N/A	N/A	1.030%	N/A	N/A	5%
6th	0.455	N/A	N/A	0.198%	N/A	N/A	5%
7th	1.856	N/A	N/A	0.807%	N/A	N/A	5%
8th	0.124	N/A	N/A	0.054%	N/A	N/A	5%
9th	1.341	N/A	N/A	0.583%	N/A	N/A	5%
10th	0.030	N/A	N/A	0.013%	N/A	N/A	5%
11th	1.058	N/A	N/A	0.460%	N/A	N/A	5%
12th	0.025	N/A	N/A	0.011%	N/A	N/A	5%
13th	0.777	N/A	N/A	0.338%	N/A	N/A	5%
14th	0.028	N/A	N/A	0.012%	N/A	N/A	5%
15th	0.591	N/A	N/A	0.257%	N/A	N/A	5%
16th	0.023	N/A	N/A	0.010%	N/A	N/A	5%
17th	0.442	N/A	N/A	0.192%	N/A	N/A	5%
18th	0.021	N/A	N/A	0.009%	N/A	N/A	5%
19th	0.343	N/A	N/A	0.149%	N/A	N/A	5%
20th	0.021	N/A	N/A	0.009%	N/A	N/A	5%
21th	0.267	N/A	N/A	0.116%	N/A	N/A	5%
22th	0.018	N/A	N/A	0.008%	N/A	N/A	5%
23th	0.216	N/A	N/A	0.094%	N/A	N/A	5%
24th	0.016	N/A	N/A	0.007%	N/A	N/A	5%
25th	0.170	N/A	N/A	0.074%	N/A	N/A	5%
26th	0.014	N/A	N/A	0.006%	N/A	N/A	5%
27th	0.152	N/A	N/A	0.066%	N/A	N/A	5%
28th	0.009	N/A	N/A	0.004%	N/A	N/A	5%
29th	0.127	N/A	N/A	0.055%	N/A	N/A	5%
30th	0.009	N/A	N/A	0.004%	N/A	N/A	5%
31th	0.104	N/A	N/A	0.045%	N/A	N/A	5%
32th	0.012	N/A	N/A	0.005%	N/A	N/A	5%
33th	0.106	N/A	N/A	0.046%	N/A	N/A	5%
34th	0.012	N/A	N/A	0.005%	N/A	N/A	5%
35th	0.074	N/A	N/A	0.032%	N/A	N/A	5%
36th	0.007	N/A	N/A	0.003%	N/A	N/A	5%
37th	0.071	N/A	N/A	0.031%	N/A	N/A	5%
38th	0.012	N/A	N/A	0.005%	N/A	N/A	5%
39th	0.064	N/A	N/A	0.028%	N/A	N/A	5%
40th	0.007	N/A	N/A	0.003%	N/A	N/A	5%
41th	0.046	N/A	N/A	0.020%	N/A	N/A	5%
42th	0.005	N/A	N/A	0.002%	N/A	N/A	5%
43th	0.044	N/A	N/A	0.019%	N/A	N/A	5%

44th	0.007	N/A	N/A	0.003%	N/A	N/A	5%
45th	0.037	N/A	N/A	0.016%	N/A	N/A	5%
46th	0.007	N/A	N/A	0.003%	N/A	N/A	5%
47th	0.025	N/A	N/A	0.011%	N/A	N/A	5%
48th	0.005	N/A	N/A	0.002%	N/A	N/A	5%
49th	0.025	N/A	N/A	0.011%	N/A	N/A	5%
50th	0.007	N/A	N/A	0.003%	N/A	N/A	5%
THD	N/A	N/A	N/A	2.390%	N/A	N/A	5%

3.4.2	Sinusoidal output in stand-alone mode- 100%Pn						P
Model: AF6K-SL							
Harmonic	$U_{harmonic}$ Value [V]			$U_{harmonic}$ of fundamental			Limit in % of fundamental
	L1 Phase	L2 Phase	L3 Phase	L1 Phase	L2 Phase	L3 Phase	
2nd	2.404	N/A	N/A	1.045%	N/A	N/A	5%
3rd	4.083	N/A	N/A	1.775%	N/A	N/A	5%
4th	1.366	N/A	N/A	0.594%	N/A	N/A	5%
5th	3.126	N/A	N/A	1.359%	N/A	N/A	5%
6th	0.656	N/A	N/A	0.285%	N/A	N/A	5%
7th	2.330	N/A	N/A	1.013%	N/A	N/A	5%
8th	0.228	N/A	N/A	0.099%	N/A	N/A	5%
9th	1.672	N/A	N/A	0.727%	N/A	N/A	5%
10th	0.087	N/A	N/A	0.038%	N/A	N/A	5%
11th	1.228	N/A	N/A	0.534%	N/A	N/A	5%
12th	0.094	N/A	N/A	0.041%	N/A	N/A	5%
13th	0.890	N/A	N/A	0.387%	N/A	N/A	5%
14th	0.099	N/A	N/A	0.043%	N/A	N/A	5%
15th	0.651	N/A	N/A	0.283%	N/A	N/A	5%
16th	0.094	N/A	N/A	0.041%	N/A	N/A	5%
17th	0.478	N/A	N/A	0.208%	N/A	N/A	5%
18th	0.085	N/A	N/A	0.037%	N/A	N/A	5%
19th	0.366	N/A	N/A	0.159%	N/A	N/A	5%
20th	0.074	N/A	N/A	0.032%	N/A	N/A	5%
21th	0.281	N/A	N/A	0.122%	N/A	N/A	5%
22th	0.064	N/A	N/A	0.028%	N/A	N/A	5%
23th	0.221	N/A	N/A	0.096%	N/A	N/A	5%
24th	0.055	N/A	N/A	0.024%	N/A	N/A	5%
25th	0.177	N/A	N/A	0.077%	N/A	N/A	5%
26th	0.048	N/A	N/A	0.021%	N/A	N/A	5%
27th	0.145	N/A	N/A	0.063%	N/A	N/A	5%
28th	0.039	N/A	N/A	0.017%	N/A	N/A	5%
29th	0.117	N/A	N/A	0.051%	N/A	N/A	5%
30th	0.037	N/A	N/A	0.016%	N/A	N/A	5%
31th	0.101	N/A	N/A	0.044%	N/A	N/A	5%
32th	0.035	N/A	N/A	0.015%	N/A	N/A	5%
33th	0.083	N/A	N/A	0.036%	N/A	N/A	5%
34th	0.030	N/A	N/A	0.013%	N/A	N/A	5%
35th	0.069	N/A	N/A	0.030%	N/A	N/A	5%
36th	0.028	N/A	N/A	0.012%	N/A	N/A	5%
37th	0.062	N/A	N/A	0.027%	N/A	N/A	5%
38th	0.023	N/A	N/A	0.010%	N/A	N/A	5%
39th	0.048	N/A	N/A	0.021%	N/A	N/A	5%
40th	0.021	N/A	N/A	0.009%	N/A	N/A	5%
41th	0.044	N/A	N/A	0.019%	N/A	N/A	5%
42th	0.021	N/A	N/A	0.009%	N/A	N/A	5%
43th	0.037	N/A	N/A	0.016%	N/A	N/A	5%

44th	0.018	N/A	N/A	0.008%	N/A	N/A	5%
45th	0.030	N/A	N/A	0.013%	N/A	N/A	5%
46th	0.014	N/A	N/A	0.006%	N/A	N/A	5%
47th	0.028	N/A	N/A	0.012%	N/A	N/A	5%
48th	0.016	N/A	N/A	0.007%	N/A	N/A	5%
49th	0.025	N/A	N/A	0.011%	N/A	N/A	5%
50th	0.014	N/A	N/A	0.006%	N/A	N/A	5%
THD	N/A	N/A	N/A	3.044%	N/A	N/A	5%
Note:							

3.4.2	Sinusoidal output in stand-alone mode- 5%Pn						**P**

Model: AF1K-SL-1

Harmonic	U_{harmonic} Value [V]			U_{harmonic} of fundamental			Limit in % of fundamental
	L1 Phase	L2 Phase	L3 Phase	L1 Phase	L2 Phase	L3 Phase	
2nd	0.161	N/A	N/A	0.070%	N/A	N/A	5%
3rd	3.556	N/A	N/A	1.546%	N/A	N/A	5%
4th	0.251	N/A	N/A	0.109%	N/A	N/A	5%
5th	2.123	N/A	N/A	0.923%	N/A	N/A	5%
6th	0.150	N/A	N/A	0.065%	N/A	N/A	5%
7th	0.895	N/A	N/A	0.389%	N/A	N/A	5%
8th	0.085	N/A	N/A	0.037%	N/A	N/A	5%
9th	0.545	N/A	N/A	0.237%	N/A	N/A	5%
10th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
11th	0.876	N/A	N/A	0.381%	N/A	N/A	5%
12th	0.156	N/A	N/A	0.068%	N/A	N/A	5%
13th	0.989	N/A	N/A	0.430%	N/A	N/A	5%
14th	0.177	N/A	N/A	0.077%	N/A	N/A	5%
15th	0.858	N/A	N/A	0.373%	N/A	N/A	5%
16th	0.186	N/A	N/A	0.081%	N/A	N/A	5%
17th	0.644	N/A	N/A	0.280%	N/A	N/A	5%
18th	0.140	N/A	N/A	0.061%	N/A	N/A	5%
19th	0.460	N/A	N/A	0.200%	N/A	N/A	5%
20th	0.117	N/A	N/A	0.051%	N/A	N/A	5%
21th	0.354	N/A	N/A	0.154%	N/A	N/A	5%
22th	0.110	N/A	N/A	0.048%	N/A	N/A	5%
23th	0.327	N/A	N/A	0.142%	N/A	N/A	5%
24th	0.108	N/A	N/A	0.047%	N/A	N/A	5%
25th	0.294	N/A	N/A	0.128%	N/A	N/A	5%
26th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
27th	0.269	N/A	N/A	0.117%	N/A	N/A	5%
28th	0.101	N/A	N/A	0.044%	N/A	N/A	5%
29th	0.232	N/A	N/A	0.101%	N/A	N/A	5%
30th	0.094	N/A	N/A	0.041%	N/A	N/A	5%
31th	0.189	N/A	N/A	0.082%	N/A	N/A	5%
32th	0.090	N/A	N/A	0.039%	N/A	N/A	5%
33th	0.175	N/A	N/A	0.076%	N/A	N/A	5%
34th	0.078	N/A	N/A	0.034%	N/A	N/A	5%
35th	0.161	N/A	N/A	0.070%	N/A	N/A	5%
36th	0.085	N/A	N/A	0.037%	N/A	N/A	5%
37th	0.143	N/A	N/A	0.062%	N/A	N/A	5%
38th	0.085	N/A	N/A	0.037%	N/A	N/A	5%
39th	0.140	N/A	N/A	0.061%	N/A	N/A	5%
40th	0.081	N/A	N/A	0.035%	N/A	N/A	5%
41th	0.138	N/A	N/A	0.060%	N/A	N/A	5%
42th	0.083	N/A	N/A	0.036%	N/A	N/A	5%
43th	0.127	N/A	N/A	0.055%	N/A	N/A	5%

44th	0.087	N/A	N/A	0.038%	N/A	N/A	5%
45th	0.115	N/A	N/A	0.050%	N/A	N/A	5%
46th	0.083	N/A	N/A	0.036%	N/A	N/A	5%
47th	0.108	N/A	N/A	0.047%	N/A	N/A	5%
48th	0.076	N/A	N/A	0.033%	N/A	N/A	5%
49th	0.099	N/A	N/A	0.043%	N/A	N/A	5%
50th	0.071	N/A	N/A	0.031%	N/A	N/A	5%
THD	N/A	N/A	N/A	2.087%	N/A	N/A	5%

3.4.2	Sinusoidal output in stand-alone mode- 50%Pn						P

Model: AF1K-SL-1

Harmonic	$U_{harmonic}$ Value [V]			$U_{harmonic}$ of fundamental			Limit in % of fundamental
	L1 Phase	L2 Phase	L3 Phase	L1 Phase	L2 Phase	L3 Phase	
2nd	0.193	N/A	N/A	0.084%	N/A	N/A	5%
3rd	3.142	N/A	N/A	1.366%	N/A	N/A	5%
4th	0.117	N/A	N/A	0.051%	N/A	N/A	5%
5th	1.451	N/A	N/A	0.631%	N/A	N/A	5%
6th	0.090	N/A	N/A	0.039%	N/A	N/A	5%
7th	0.235	N/A	N/A	0.102%	N/A	N/A	5%
8th	0.074	N/A	N/A	0.032%	N/A	N/A	5%
9th	0.600	N/A	N/A	0.261%	N/A	N/A	5%
10th	0.122	N/A	N/A	0.053%	N/A	N/A	5%
11th	0.823	N/A	N/A	0.358%	N/A	N/A	5%
12th	0.159	N/A	N/A	0.069%	N/A	N/A	5%
13th	0.685	N/A	N/A	0.298%	N/A	N/A	5%
14th	0.090	N/A	N/A	0.039%	N/A	N/A	5%
15th	0.389	N/A	N/A	0.169%	N/A	N/A	5%
16th	0.083	N/A	N/A	0.036%	N/A	N/A	5%
17th	0.198	N/A	N/A	0.086%	N/A	N/A	5%
18th	0.069	N/A	N/A	0.030%	N/A	N/A	5%
19th	0.345	N/A	N/A	0.150%	N/A	N/A	5%
20th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
21th	0.398	N/A	N/A	0.173%	N/A	N/A	5%
22th	0.127	N/A	N/A	0.055%	N/A	N/A	5%
23th	0.327	N/A	N/A	0.142%	N/A	N/A	5%
24th	0.104	N/A	N/A	0.045%	N/A	N/A	5%
25th	0.255	N/A	N/A	0.111%	N/A	N/A	5%
26th	0.090	N/A	N/A	0.039%	N/A	N/A	5%
27th	0.262	N/A	N/A	0.114%	N/A	N/A	5%
28th	0.104	N/A	N/A	0.045%	N/A	N/A	5%
29th	0.274	N/A	N/A	0.119%	N/A	N/A	5%
30th	0.131	N/A	N/A	0.057%	N/A	N/A	5%
31th	0.239	N/A	N/A	0.104%	N/A	N/A	5%
32th	0.115	N/A	N/A	0.050%	N/A	N/A	5%
33th	0.232	N/A	N/A	0.101%	N/A	N/A	5%
34th	0.097	N/A	N/A	0.042%	N/A	N/A	5%
35th	0.221	N/A	N/A	0.096%	N/A	N/A	5%
36th	0.122	N/A	N/A	0.053%	N/A	N/A	5%
37th	0.193	N/A	N/A	0.084%	N/A	N/A	5%
38th	0.117	N/A	N/A	0.051%	N/A	N/A	5%
39th	0.196	N/A	N/A	0.085%	N/A	N/A	5%
40th	0.094	N/A	N/A	0.041%	N/A	N/A	5%
41th	0.175	N/A	N/A	0.076%	N/A	N/A	5%
42th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
43th	0.136	N/A	N/A	0.059%	N/A	N/A	5%

44th	0.110	N/A	N/A	0.048%	N/A	N/A	5%
45th	0.133	N/A	N/A	0.058%	N/A	N/A	5%
46th	0.081	N/A	N/A	0.035%	N/A	N/A	5%
47th	0.131	N/A	N/A	0.057%	N/A	N/A	5%
48th	0.076	N/A	N/A	0.033%	N/A	N/A	5%
49th	0.101	N/A	N/A	0.044%	N/A	N/A	5%
50th	0.090	N/A	N/A	0.039%	N/A	N/A	5%
THD	N/A	N/A	N/A	1.710%	N/A	N/A	5%

3.4.2	Sinusoidal output in stand-alone mode- 100%Pn						**P**
Model: AF1K-SL-1							
Harmonic	Value V			$U_{harmonic}$ of fundamental			Limit in % of fundamental
	L1 Phase	L2 Phase	L3 Phase	L1 Phase	L2 Phase	L3 Phase	
2nd	0.193	N/A	N/A	0.084%	N/A	N/A	5%
3rd	2.732	N/A	N/A	1.188%	N/A	N/A	5%
4th	0.145	N/A	N/A	0.063%	N/A	N/A	5%
5th	1.766	N/A	N/A	0.768%	N/A	N/A	5%
6th	0.127	N/A	N/A	0.055%	N/A	N/A	5%
7th	1.270	N/A	N/A	0.552%	N/A	N/A	5%
8th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
9th	0.911	N/A	N/A	0.396%	N/A	N/A	5%
10th	0.094	N/A	N/A	0.041%	N/A	N/A	5%
11th	0.547	N/A	N/A	0.238%	N/A	N/A	5%
12th	0.081	N/A	N/A	0.035%	N/A	N/A	5%
13th	0.331	N/A	N/A	0.144%	N/A	N/A	5%
14th	0.039	N/A	N/A	0.017%	N/A	N/A	5%
15th	0.154	N/A	N/A	0.067%	N/A	N/A	5%
16th	0.053	N/A	N/A	0.023%	N/A	N/A	5%
17th	0.064	N/A	N/A	0.028%	N/A	N/A	5%
18th	0.039	N/A	N/A	0.017%	N/A	N/A	5%
19th	0.081	N/A	N/A	0.035%	N/A	N/A	5%
20th	0.041	N/A	N/A	0.018%	N/A	N/A	5%
21th	0.108	N/A	N/A	0.047%	N/A	N/A	5%
22th	0.053	N/A	N/A	0.023%	N/A	N/A	5%
23th	0.131	N/A	N/A	0.057%	N/A	N/A	5%
24th	0.055	N/A	N/A	0.024%	N/A	N/A	5%
25th	0.147	N/A	N/A	0.064%	N/A	N/A	5%
26th	0.051	N/A	N/A	0.022%	N/A	N/A	5%
27th	0.138	N/A	N/A	0.060%	N/A	N/A	5%
28th	0.051	N/A	N/A	0.022%	N/A	N/A	5%
29th	0.129	N/A	N/A	0.056%	N/A	N/A	5%
30th	0.055	N/A	N/A	0.024%	N/A	N/A	5%
31th	0.113	N/A	N/A	0.049%	N/A	N/A	5%
32th	0.053	N/A	N/A	0.023%	N/A	N/A	5%
33th	0.104	N/A	N/A	0.045%	N/A	N/A	5%
34th	0.044	N/A	N/A	0.019%	N/A	N/A	5%
35th	0.078	N/A	N/A	0.034%	N/A	N/A	5%
36th	0.058	N/A	N/A	0.025%	N/A	N/A	5%
37th	0.099	N/A	N/A	0.043%	N/A	N/A	5%
38th	0.046	N/A	N/A	0.020%	N/A	N/A	5%
39th	0.083	N/A	N/A	0.036%	N/A	N/A	5%
40th	0.037	N/A	N/A	0.016%	N/A	N/A	5%
41th	0.076	N/A	N/A	0.033%	N/A	N/A	5%
42th	0.055	N/A	N/A	0.024%	N/A	N/A	5%
43th	0.067	N/A	N/A	0.029%	N/A	N/A	5%

44th	0.051	N/A	N/A	0.022%	N/A	N/A	5%
45th	0.074	N/A	N/A	0.032%	N/A	N/A	5%
46th	0.032	N/A	N/A	0.014%	N/A	N/A	5%
47th	0.078	N/A	N/A	0.034%	N/A	N/A	5%
48th	0.039	N/A	N/A	0.017%	N/A	N/A	5%
49th	0.044	N/A	N/A	0.019%	N/A	N/A	5%
50th	0.053	N/A	N/A	0.023%	N/A	N/A	5%
THD	N/A	N/A	N/A	1.647%	N/A	N/A	5%
Note:							

Appendix B	TABLE: Harmonic Voltage			P
Order	Phase L1 U_h(%)	Phase L2 U_h(%)	Phase L2 U_h(%)	Limited (%)
2	0.005	-	-	0.2
3	0.519	-	-	0.9
4	0.011	-	-	0.2
5	0.165	-	-	0.4
6	0.009	-	-	0.2
7	0.090	-	-	0.3
8	0.003	-	-	0.2
9	0.038	-	-	0.2
10	0.003	-	-	0.2
11	0.043	-	-	0.1
12	0.004	-	-	0.1
13	0.080	-	-	0.1
14	0.004	-	-	0.1
15	0.030	-	-	0.1
16	0.001	-	-	0.1
17	0.019	-	-	0.1
18	0.003	-	-	0.1
19	0.015	-	-	0.1
20	0.002	-	-	0.1
21	0.007	-	-	0.1
22	0.002	-	-	0.1
23	0.006	-	-	0.1
24	0.001	-	-	0.1
25	0.005	-	-	0.1
26	0.001	-	-	0.1
27	0.012	-	-	0.1
28	0.001	-	-	0.1
29	0.004	-	-	0.1
30	0.001	-	-	0.1
31	0.008	-	-	0.1
32	0.002	-	-	0.1
33	0.001	-	-	0.1
34	0.001	-	-	0.1
35	0.004	-	-	0.1
36	0.001	-	-	0.1
37	0.001	-	-	0.1
38	0.001	-	-	0.1
39	0.007	-	-	0.1
40	0.001	-	-	0.1
41	0.002	-	-	0.1
42	0.001	-	-	0.1
43	0.005	-	-	0.1
44	0.002	-	-	0.1
45	0.003	-	-	0.1
46	0.001	-	-	0.1
47	0.005	-	-	0.1
48	0.001	-	-	0.1
49	0.006	-	-	0.1
50	0.001	-	-	0.1
THD (%)	0.563	-	-	5

Appendix B		TABLE: Harmonic current limit test—100%In						P
Model		AF6K-SL						
Harmonic		L1		L2		L3		Limits -%In
Order	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	-	
02	0.042	0.159	--	--	--	--	1%
03	0.431	1.653	--	--	--	--	4%
04	0.009	0.033	--	--	--	--	1%
05	0.280	1.073	--	--	--	--	4%
06	0.012	0.046	--	--	--	--	1%
07	0.211	0.809	--	--	--	--	4%
08	0.007	0.026	--	--	--	--	1%
09	0.161	0.616	--	--	--	--	2%
10	0.010	0.039	--	--	--	--	0.5%
11	0.132	0.507	--	--	--	--	2%
12	0.003	0.010	--	--	--	--	0.5%
13	0.099	0.380	--	--	--	--	2%
14	0.003	0.012	--	--	--	--	0.5%
15	0.072	0.275	--	--	--	--	1%
16	0.002	0.006	--	--	--	--	0.5%
17	0.056	0.213	--	--	--	--	1.5%
18	0.004	0.015	--	--	--	--	0.5%
19	0.044	0.170	--	--	--	--	1.5%
20	0.003	0.012	--	--	--	--	0.5%
21	0.037	0.142	--	--	--	--	0.6%
22	0.002	0.006	--	--	--	--	0.5%
23	0.032	0.123	--	--	--	--	0.6%
24	0.002	0.007	--	--	--	--	0.5%
25	0.031	0.118	--	--	--	--	0.6%
26	0.003	0.010	--	--	--	--	0.5%
27	0.026	0.099	--	--	--	--	0.6%
28	0.002	0.007	--	--	--	--	0.5%
29	0.025	0.095	--	--	--	--	0.6%
30	0.002	0.007	--	--	--	--	0.5%
31	0.023	0.087	--	--	--	--	0.6%
32	0.001	0.005	--	--	--	--	0.5%
33	0.019	0.072	--	--	--	--	0.6%
34	0.002	0.006	--	--	--	--	--
35	0.017	0.066	--	--	--	--	--
36	0.002	0.007	--	--	--	--	--
37	0.017	0.066	--	--	--	--	--
38	0.001	0.005	--	--	--	--	--
39	0.015	0.056	--	--	--	--	--
40	0.002	0.007	--	--	--	--	--
41	0.013	0.050	--	--	--	--	--
42	0.002	0.007	--	--	--	--	--
43	0.013	0.049	--	--	--	--	--
44	0.001	0.005	--	--	--	--	--
45	0.011	0.043	--	--	--	--	--
46	0.001	0.005	--	--	--	--	--
47	0.009	0.036	--	--	--	--	--
48	0.002	0.006	--	--	--	--	--
49	0.009	0.034	--	--	--	--	--
50	0.001	0.005	--	--	--	--	--
A total	--	2.717	--	--	--	--	5.0%

Appendix B	TABLE: Harmonic current limit test—50%In						P
Model	AF6K-SL						
Harmonic	L1		L2		L3		Limits -%In
Order	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	-
02	0.095	0.363	--	--	--	--	1%
03	0.261	0.999	--	--	--	--	4%
04	0.016	0.062	--	--	--	--	1%
05	0.226	0.865	--	--	--	--	4%
06	0.002	0.008	--	--	--	--	1%
07	0.187	0.717	--	--	--	--	4%
08	0.006	0.023	--	--	--	--	1%
09	0.109	0.418	--	--	--	--	2%
10	0.001	0.005	--	--	--	--	0.5%
11	0.092	0.353	--	--	--	--	2%
12	0.002	0.006	--	--	--	--	0.5%
13	0.079	0.304	--	--	--	--	2%
14	0.002	0.007	--	--	--	--	0.5%
15	0.060	0.231	--	--	--	--	1%
16	0.002	0.007	--	--	--	--	0.5%
17	0.046	0.174	--	--	--	--	1.5%
18	0.001	0.004	--	--	--	--	0.5%
19	0.037	0.140	--	--	--	--	1.5%
20	0.001	0.004	--	--	--	--	0.5%
21	0.031	0.119	--	--	--	--	0.6%
22	0.002	0.007	--	--	--	--	0.5%
23	0.025	0.094	--	--	--	--	0.6%
24	0.001	0.005	--	--	--	--	0.5%
25	0.016	0.061	--	--	--	--	0.6%
26	0.001	0.004	--	--	--	--	0.5%
27	0.014	0.053	--	--	--	--	0.6%
28	0.001	0.002	--	--	--	--	0.5%
29	0.010	0.038	--	--	--	--	0.6%
30	0.001	0.002	--	--	--	--	0.5%
31	0.007	0.026	--	--	--	--	0.6%
32	0.001	0.005	--	--	--	--	0.5%
33	0.005	0.017	--	--	--	--	0.6%
34	0.001	0.002	--	--	--	--	--
35	0.007	0.026	--	--	--	--	--
36	0.001	0.002	--	--	--	--	--
37	0.006	0.024	--	--	--	--	--
38	0.001	0.003	--	--	--	--	--
39	0.007	0.027	--	--	--	--	--
40	0.001	0.003	--	--	--	--	--
41	0.007	0.027	--	--	--	--	--
42	0.001	0.003	--	--	--	--	--
43	0.008	0.029	--	--	--	--	--
44	0.001	0.003	--	--	--	--	--
45	0.008	0.029	--	--	--	--	--
46	0.000	0.002	--	--	--	--	--
47	0.007	0.027	--	--	--	--	--
48	0.001	0.005	--	--	--	--	--
49	0.007	0.025	--	--	--	--	--
50	0.001	0.002	--	--	--	--	--

Appendix B	TABLE: Harmonic current limit test—50%In						P
Model	AF6K-SL						
Harmonic	L1		L2		L3		Limits -%In
Order	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	-
A total	--	3.583	--	--	--	--	5.0%

Appendix B	TABLE: Harmonic current limit test—100%In						P
Model	AF1K-SL-1						
Harmonic	L1		L2		L3		Limits -%In
Order	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	-
02	0.025	0.573	--	--	--	--	1%
03	0.077	1.778	--	--	--	--	4%
04	0.004	0.086	--	--	--	--	1%
05	0.059	1.352	--	--	--	--	4%
06	0.001	0.029	--	--	--	--	1%
07	0.051	1.173	--	--	--	--	4%
08	0.002	0.056	--	--	--	--	1%
09	0.033	0.755	--	--	--	--	2%
10	0.000	0.010	--	--	--	--	0.5%
11	0.024	0.542	--	--	--	--	2%
12	0.000	0.008	--	--	--	--	0.5%
13	0.020	0.469	--	--	--	--	2%
14	0.001	0.015	--	--	--	--	0.5%
15	0.016	0.378	--	--	--	--	1%
16	0.001	0.027	--	--	--	--	0.5%
17	0.013	0.309	--	--	--	--	1.5%
18	0.001	0.011	--	--	--	--	0.5%
19	0.011	0.262	--	--	--	--	1.5%
20	0.001	0.014	--	--	--	--	0.5%
21	0.009	0.196	--	--	--	--	0.6%
22	0.001	0.017	--	--	--	--	0.5%
23	0.009	0.214	--	--	--	--	0.6%
24	0.000	0.006	--	--	--	--	0.5%
25	0.006	0.144	--	--	--	--	0.6%
26	0.000	0.006	--	--	--	--	0.5%
27	0.006	0.130	--	--	--	--	0.6%
28	0.000	0.007	--	--	--	--	0.5%
29	0.005	0.116	--	--	--	--	0.6%
30	0.000	0.006	--	--	--	--	0.5%
31	0.003	0.077	--	--	--	--	0.6%
32	0.001	0.014	--	--	--	--	0.5%
33	0.004	0.099	--	--	--	--	0.6%
34	0.000	0.008	--	--	--	--	--
35	0.002	0.055	--	--	--	--	--
36	0.000	0.003	--	--	--	--	--
37	0.002	0.051	--	--	--	--	--
38	0.000	0.007	--	--	--	--	--
39	0.001	0.028	--	--	--	--	--
40	0.000	0.008	--	--	--	--	--
41	0.002	0.050	--	--	--	--	--
42	0.000	0.006	--	--	--	--	--
43	0.001	0.029	--	--	--	--	--
44	0.000	0.008	--	--	--	--	--
45	0.002	0.042	--	--	--	--	--
46	0.000	0.004	--	--	--	--	--
47	0.002	0.044	--	--	--	--	--
48	0.000	0.004	--	--	--	--	--
49	0.002	0.040	--	--	--	--	--
50	0.000	0.005	--	--	--	--	--
A total	--	3.044	--	--	--	--	5.0%

Appendix B	TABLE: Harmonic current limit test—50%In						P
Model	AF1K-SL-1						
Harmonic	L1		L2		L3		Limits -%In
Order	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	-
02	0.020	0.456	--	--	--	--	1%
03	0.063	1.410	--	--	--	--	4%
04	0.004	0.082	--	--	--	--	1%
05	0.056	1.261	--	--	--	--	4%
06	0.000	0.008	--	--	--	--	1%
07	0.037	0.832	--	--	--	--	4%
08	0.001	0.017	--	--	--	--	1%
09	0.027	0.597	--	--	--	--	2%
10	0.000	0.008	--	--	--	--	0.5%
11	0.018	0.402	--	--	--	--	2%
12	0.000	0.009	--	--	--	--	0.5%
13	0.012	0.262	--	--	--	--	2%
14	0.001	0.013	--	--	--	--	0.5%
15	0.009	0.197	--	--	--	--	1%
16	0.001	0.011	--	--	--	--	0.5%
17	0.006	0.135	--	--	--	--	1.5%
18	0.000	0.009	--	--	--	--	0.5%
19	0.004	0.090	--	--	--	--	1.5%
20	0.000	0.008	--	--	--	--	0.5%
21	0.002	0.044	--	--	--	--	0.6%
22	0.001	0.011	--	--	--	--	0.5%
23	0.001	0.027	--	--	--	--	0.6%
24	0.000	0.005	--	--	--	--	0.5%
25	0.001	0.025	--	--	--	--	0.6%
26	0.000	0.006	--	--	--	--	0.5%
27	0.001	0.018	--	--	--	--	0.6%
28	0.000	0.003	--	--	--	--	0.5%
29	0.001	0.022	--	--	--	--	0.6%
30	0.000	0.003	--	--	--	--	0.5%
31	0.001	0.014	--	--	--	--	0.6%
32	0.000	0.004	--	--	--	--	0.5%
33	0.001	0.026	--	--	--	--	0.6%
34	0.000	0.006	--	--	--	--	--
35	0.001	0.015	--	--	--	--	--
36	0.000	0.004	--	--	--	--	--
37	0.001	0.022	--	--	--	--	--
38	0.000	0.003	--	--	--	--	--
39	0.001	0.023	--	--	--	--	--
40	0.000	0.007	--	--	--	--	--
41	0.002	0.049	--	--	--	--	--
42	0.000	0.003	--	--	--	--	--
43	0.002	0.044	--	--	--	--	--
44	0.000	0.002	--	--	--	--	--
45	0.002	0.043	--	--	--	--	--
46	0.000	0.007	--	--	--	--	--
47	0.003	0.058	--	--	--	--	--
48	0.000	0.003	--	--	--	--	--
49	0.002	0.045	--	--	--	--	--

Appendix B	TABLE: Harmonic current limit test—50%In						P
Model	AF1K-SL-1						
Harmonic	L1		L2		L3		Limits -%In
Order	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	Magnitude (A)	% of Fundamental	-
50	0.000	0.002	--	--	--	--	--
A total	--	4.823	--	--	--	--	5.0%

Additional	TABLE: Voltage fluctuations and flicker				P

Model AF6K-SL

Parameter	Limit value	Result		
		L1	L2	L3
Plt	0,65(12)	0.17	--	--
Pst	1,00	0.19	--	--
dc(%)	3,3%	0.38	--	--
d max (%)	4%	0.70	--	--
d(t)%	3,3%(500ms)	0	--	--

Impedance: $Z_L = 0.15Ω+j0.15Ω$, $Z_N = 0.10Ω +j0.10Ω$

Model AF1K-SL-1

Parameter	Limit value	Result		
		L1	L2	L3
Plt	0,65(12)	0.17	--	--
Pst	1,00	0.19	--	--
dc(%)	3,3%	0.24	--	--
d max (%)	4%	0.71	--	--
d(t)%	3,3%(500ms)	0	--	--

Impedance: $Z_L = 0.24Ω+j0.15Ω$, $Z_N = 0.16Ω+j0.10Ω$

Appendix C	TABLE: Transient Voltage limit test			P
Phase L1				

		Test output apparent power [VA]		
Duration [s]	Transient Voltage Limits [V]	10% output	50% output	100% output
		600	3000	6000
		Measurements of Instantaneous Voltage (Line to Neutral) [V] for Phase L1		
0.0002	910	394.5	325.1	323.1
0.0006	710	394.1	320.9	304.9
0.002	580	381.3	310.4	304.5
0.006	470	314.8	309.1	302.5
0.02	420	306.9	305.0	295.4
0.06	390	285.1	282.6	274.1
0.2	390	216.5	216.1	208.2
0.6	390	88.2	88.4	84.1

Measurements of transient voltage curve (Line to Neutral)
10%output
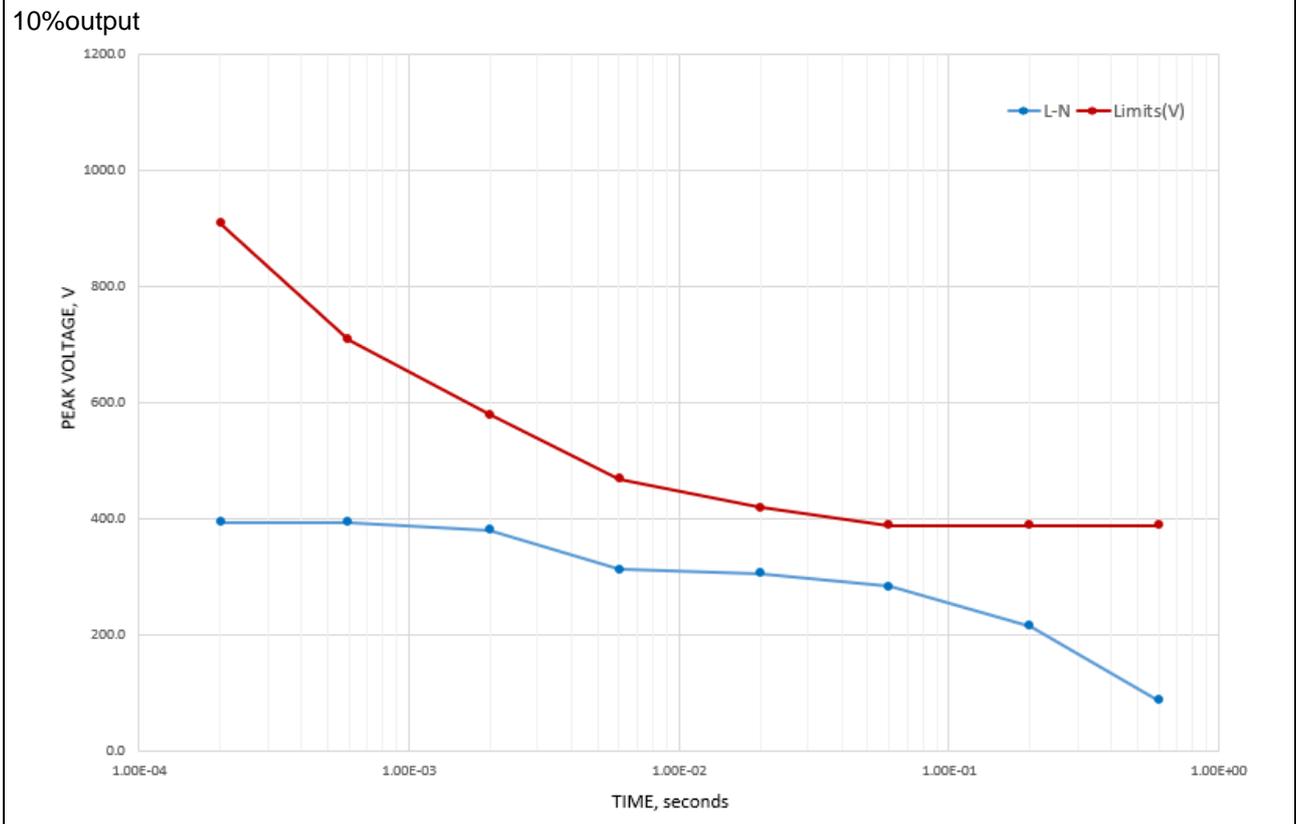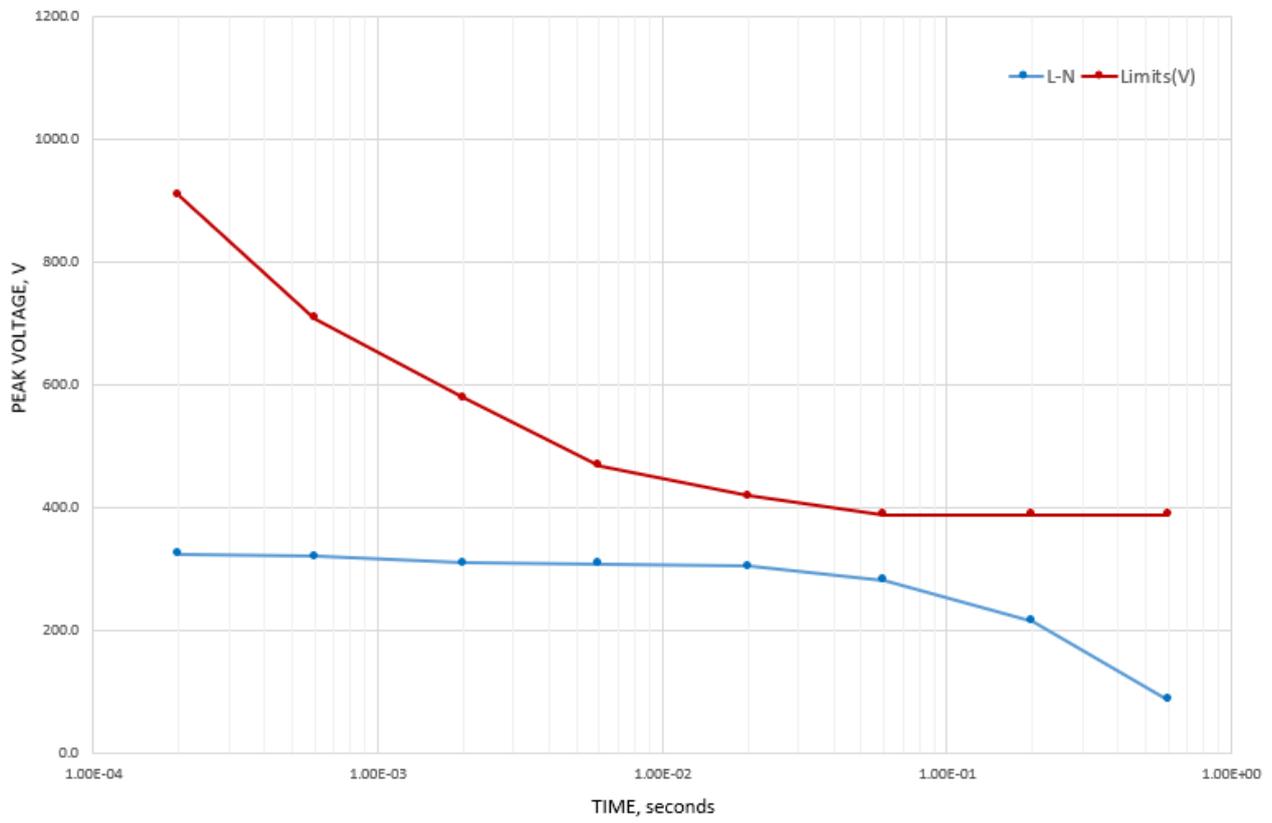
50% output

100% output
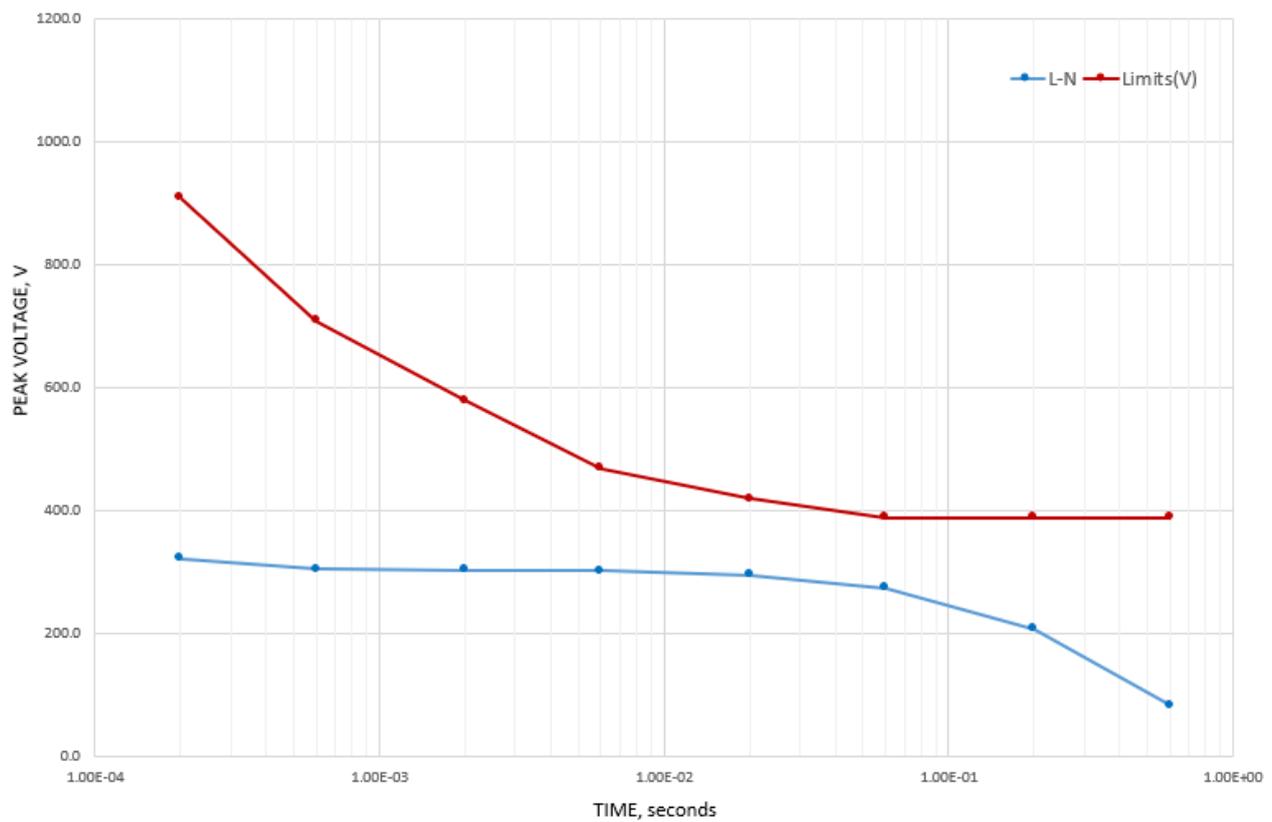
Appendix D	TABLE: DC Injection test			P
Model	AF6K-SL			
Test Conditions I/In	Measurements			Limit
	Idc / In [%]			Idc/In
	L1	L2	L3	
20%	0.02	--	--	0.5%
60%	0.01	--	--	0.5%
100%	0.02	--	--	0.5%
Note(s):				

Appendix D	TABLE: DC Injection test			P
Model	AF1K-SL-1			
Test Conditions I/In	Measurements			Limit
	Idc / In [%]			Idc/In
	L1	L2	L3	
20%	0.03	--	--	0.5%
60%	0.12	--	--	0.5%
100%	0.13	--	--	0.5%
Note(s):				

Appendix E	TABLE: Demand Response Modes Testing including disconnection on external signal	P
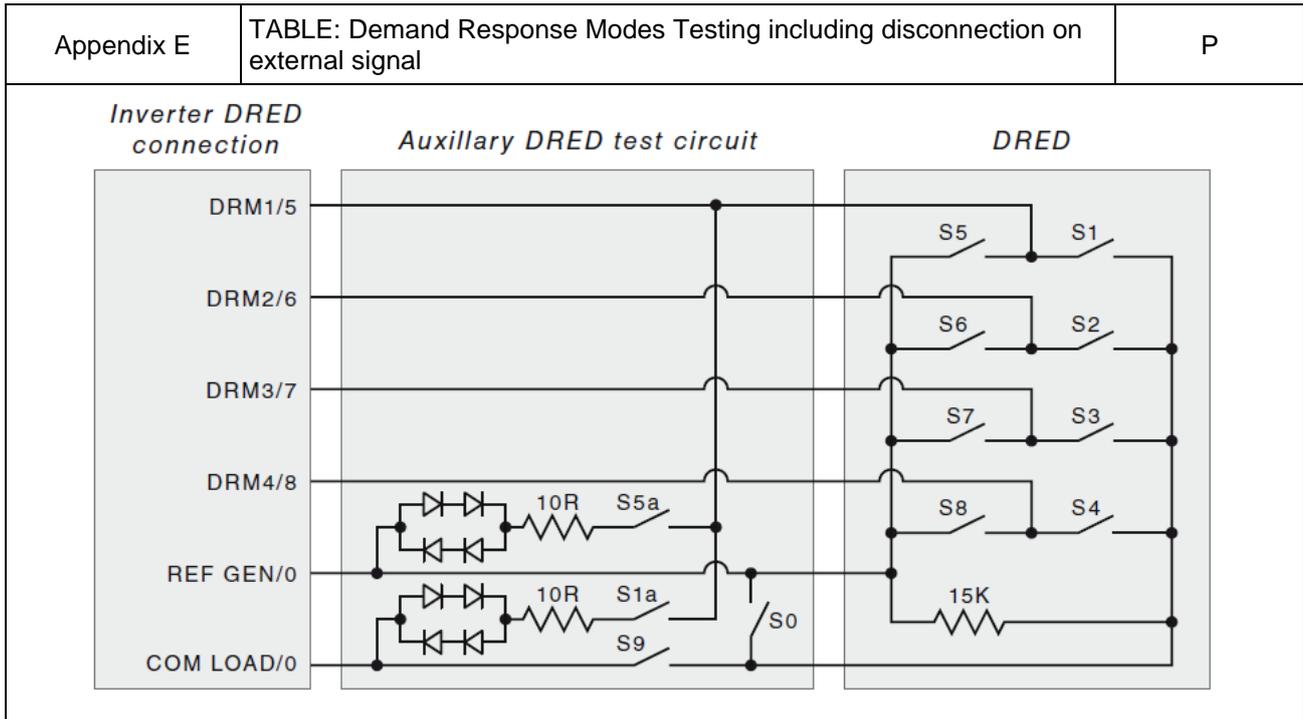
	Voltage(V) Max.	Current(mA) Max.
S1-S8 and S0 on (limit 30mA, 0.1V)	0.03	0
S1a, S5a (limit 30mA, 1.5-1.6V)	0.8	0

Demand response test	Real current		Reactive current		Switching time	Pass/Fail
	Value	Ia/In	Value	Iq/In		
DRM 0 at 100%	0	0	0.178	0.7%	1.15s	Pass
DRM 7	--	--	--	--	--	--
DRM 6 and DRM 7	--	--	--	--	--	--
DRM 6	--	--	--	--	--	--
DRM 5 andDRM 6	--	--	--	--	--	--
DRM 8	--	--	--	--	--	--
DRM 3	--	--	--	--	--	--
DRM3 and DRM 2	--	--	--	--	--	--
DRM2	--	--	--	--	--	--
DRM1 and DRM2	--	--	--	--	--	--
DRM4	--	--	--	--	--	--

Appendix F.1.1	TABLE: Fixed power factor mode								P
Model	AF6K-SL								
Test Conditions	Measurements							Target value	Limit
I/In	cosφ	P / Sn	Q / Sn	I/In	cosφ	Δ cosφ	leading / lagging	cosφ	cosφ
25%	1.0	25.0%	1.6%	25.1%	0.998	-0.002	--	1.0	±0.01
50%	1.0	50.1%	1.8%	50.1%	0.999	-0.001	--	1.0	±0.01
75%	1.0	75.0%	1.7%	75.0%	0.999	-0.001	--	1.0	±0.01
100%	1.0	99.9%	1.8%	99.9%	0.999	-0.001	--	1.0	±0.01
25%	0.8	20.2%	15.1%	25.2%	0.801	0.001	leading	0.8	±0.01
50%	0.8	40.1%	29.9%	50.0%	0.801	0.001	leading	0.8	±0.01
75%	0.8	60.1%	45.0%	75.1%	0.801	0.001	leading	0.8	±0.01
100%	0.8	80.0%	60.0%	100.0%	0.800	0.000	leading	0.8	±0.01
25%	-0.8	-20.0%	15.0%	25.0%	-0.800	0.000	lagging	-0.8	±0.01
50%	-0.8	-40.1%	30.0%	50.1%	-0.801	0.000	lagging	-0.8	±0.01
75%	-0.8	-60.0%	45.0%	75.0%	-0.800	0.000	lagging	-0.8	±0.01
100%	-0.8	-80.0%	59.8%	99.9%	-0.801	-0.001	lagging	-0.8	±0.01
Note(s):									

Appendix F.1.1	TABLE: Fixed power factor mode								P
Model	AF1K-SL-1								
Test Conditions	Measurements							Target value	Limit
I/In	cosφ	P / Sn	Q / Sn	I/In	cosφ	Δ cosφ	leading / lagging	cosφ	cosφ
25%	1.0	25.0%	1.9%	25.0%	0.998	-0.002	--	1.0	±0.01
50%	1.0	50.0%	1.8%	50.0%	0.999	-0.001	--	1.0	±0.01
75%	1.0	74.9%	1.7%	75.0%	0.999	-0.001	--	1.0	±0.01
100%	1.0	99.9%	1.8%	99.9%	0.999	-0.001	--	1.0	±0.01
25%	0.8	20.1%	15.1%	25.1%	0.800	0.000	leading	0.8	±0.01
50%	0.8	40.1%	30.0%	50.1%	0.801	0.001	leading	0.8	±0.01
75%	0.8	60.0%	45.0%	75.0%	0.800	0.000	leading	0.8	±0.01
100%	0.8	80.1%	59.9%	100.0%	0.801	0.001	leading	0.8	±0.01
25%	-0.8	-20.1%	15.1%	25.1%	-0.800	0.000	lagging	-0.8	±0.01
50%	-0.8	-40.0%	30.0%	50.0%	-0.800	0.000	lagging	-0.8	±0.01
75%	-0.8	-60.1%	44.9%	75.0%	-0.801	-0.001	lagging	-0.8	±0.01
100%	-0.8	-80.1%	59.9%	100.0%	-0.801	-0.001	lagging	-0.8	±0.01
Note(s):									

Appendix F.1.2	TABLE: Fixed reactive power mode							P
Model	AF6K-SL							
Test Conditions		Measurements					Target value	Limit
P/Sn	Q/Sn	P / Sn	Q / Sn	cosφ	∆Q/Sn	leading / lagging	Q/Sn	∆Q/Sn
20%	60%	20.2%	60.3%	0.3179	0.30%	leading	60%	±4%
60%	60%	60.8%	59.5%	0.7147	0.50%	leading	60%	±4%
80%	60%	80.3%	59.2%	0.8049	0.80%	leading	60%	±4%
20%	-60%	20.8%	-58.7%	-0.3336	1.30%	lagging	-60%	±4%
60%	-60%	60.5%	-59.5%	-0.7125	0.50%	lagging	-60%	±4%
80%	-60%	80.2%	-59.8%	-0.8013	0.20%	lagging	-60%	±4%
Note(s):								

Appendix F.1.2	TABLE: Fixed reactive power mode							P
Model	AF1K-SL-1							
Test Conditions		Measurements					Target value	Limit
P/Sn	Q/Sn	P / Sn	Q / Sn	cosφ	∆Q/Sn	leading / lagging	Q/Sn	∆Q/Sn
20%	60%	20.5%	61.0%	0.3184	1.00%	leading	60%	±4%
60%	60%	61.0%	61.0%	0.7072	1.00%	leading	60%	±4%
80%	60%	80.3%	60.4%	0.7990	0.40%	leading	60%	±4%
20%	-60%	20.5%	-60.8%	-0.3195	0.80%	lagging	-60%	±4%
60%	-60%	60.0%	-60.7%	-0.7033	0.70%	lagging	-60%	±4%
80%	-60%	80.5%	-61.5%	-0.7946	1.50%	lagging	-60%	±4%
Note(s):								

Appendix G.2.1	TABLE: Volt-wat response mode (enable by default)						P

Model AF6K-SL							

P(U) curve settings: Australia A	Points		Vw1			Vw2	
	U [V]		253			260	
	P/Sn		100%			20%	

P(U) function	Enable
Q(U) function	Disabled

Test Conditions	Measurements					Limits	
U [V]	U [V]	P / Sn	$T_{settling}$ [s]	Q / Sn	S/Sn	P / Sn	$T_{settling}$ [s]
230, ≥20s	230.01	99.99%	--	2.01%	99.99%	100%±5%	--
253, ≥20s	253.00	99.99%	0.10	1.82%	99.99%	≤ 100%	≤ 10
254.2, ≥20s	254.21	85.49%	0.60	1.81%	85.49%	≤ 86%	≤ 10
255.4, ≥20s	255.40	72.44%	0.80	1.75%	72.44%	≤ 73%	≤ 10
256.6, ≥20s	256.61	58.38%	0.80	1.70%	58.38%	≤ 59%	≤ 10
257.8, ≥20s	257.80	44.26%	0.80	1.64%	44.26%	≤ 45%	≤ 10
259, ≥20s	259.01	30.37%	0.80	1.60%	30.37%	≤ 31%	≤ 10
257.8, ≥20s	257.80	44.73%	0.80	1.64%	44.73%	≤ 45%	≤ 10
256.6, ≥20s	256.61	58.68%	0.80	1.70%	58.68%	≤ 59%	≤ 10
255.4, ≥20s	255.41	72.24%	0.80	1.75%	72.24%	≤ 73%	≤ 10
254.2, ≥20s	254.20	85.35%	0.80	1.81%	85.35%	≤ 86%	≤ 10
253, ≥20s	253.10	99.93%	0.60	1.83%	99.93%	≤ 100%	≤ 10
259, ≥20s	259.12	30.02%	1.40	1.61%	30.02%	≤ 31%	≤ 10

Following configuration shall be inspected				
Australia A	Available / ~~Not available~~	Australia B		Available / ~~Not available~~
Australia C	Available / ~~Not available~~	New Zealand		Available / ~~Not available~~
P(U) Configurable range	Points	Vw1		Vw2
	U [V]	235-255		240-265
	P/Sn	100%		0-20%

Note(s):

Plotting

Appendix G.2.1	TABLE: Volt-wat response mode (enable by default)						P
Model AF1K-SL-1							

P(U) curve settings: Australia A	Points		Vw1			Vw2	
	U [V]		253			260	
	P/Sn		100%			20%	

P(U) function	Enable
Q(U) function	Disabled

Test Conditions	Measurements					Limits	
U [V]	U [V]	P / Sn	$T_{settling}$ [s]	Q / Sn	S/Sn	P / Sn	$T_{settling}$ [s]
230, ≥20s	230.03	100.00%	--	2.73%	100.00%	100%±5%	--
253, ≥20s	253.01	99.99%	0.10	2.47%	99.99%	≤ 100%	≤ 10
254.2, ≥20s	254.21	85.36%	1.00	2.43%	85.36%	≤ 86%	≤ 10
255.4, ≥20s	255.41	72.13%	0.80	2.36%	72.13%	≤ 73%	≤ 10
256.6, ≥20s	256.61	57.99%	0.80	2.29%	57.99%	≤ 59%	≤ 10
257.8, ≥20s	257.81	44.03%	0.80	2.21%	44.03%	≤ 45%	≤ 10
259, ≥20s	259.04	30.22%	0.80	2.15%	30.22%	≤ 31%	≤ 10
257.8, ≥20s	257.80	44.11%	0.80	2.21%	44.11%	≤ 45%	≤ 10
256.6, ≥20s	256.61	58.12%	1.00	2.29%	58.12%	≤ 59%	≤ 10
255.4, ≥20s	255.41	72.22%	1.20	2.37%	72.22%	≤ 73%	≤ 10
254.2, ≥20s	254.21	85.76%	1.00	2.43%	85.76%	≤ 86%	≤ 10
253, ≥20s	253.00	99.99%	1.20	2.47%	99.99%	≤ 100%	≤ 10
259, ≥20s	259.08	30.11%	1.20	2.19%	30.11%	≤ 31%	≤ 10

Following configuration shall be inspected				
Australia A	Available / ~~Not available~~	Australia B		Available / ~~Not available~~
Australia C	Available / ~~Not available~~	New Zealand		Available / ~~Not available~~

P(U) Configurable range	Points	Vw1	Vw2
	U [V]	235-255	240-265
	P/Sn	100%	0-20%

Note(s):

Plotting

Appendix G.2.2	TABLE: Combined volt-var and volt-watt response modes (enable by default)									P

Model AF6K-SL

P(U) curve settings: Australia A	Points				Vw1				Vw2	
	U [V]				253				260	
	P/Sn				100%				20%	

Q(U) curve settings: Australia A	Points			Vv1		Vv2		Vv3		Vv4
	U [V]			207		220		240		258
	Q/Sn			44%		0%		0%		-60%

Q(U) function (priority)				Enabled						

P(U) function				Enabled						

Test Conditions	Measurements						Target	Limits		
U [V]	U [V]	P/Sn [%]	$T_{settling}$ [s]	Q/Sn [%]	ΔQ/Sn [%]	$T_{settling}$ [s]	Q/Sn	P / Sn	ΔQ / Sn	$T_{settling}$ [s]
230, ≥20s	230.04	100.00	0.20	1.89	0.02	0.20	0%	100%±5%	--	--
240, ≥20s	240.01	99.86	0.80	1.84	0.02	0.80	0%	≤ 100%	≤ ±4%	≤ 10
243.6, ≥20s	243.61	98.81	1.40	-13.61	-0.02	1.60	-12%	≤ 99%	≤ ±4%	≤ 10
247.2, ≥20s	247.21	96.49	1.40	-24.98	-0.01	1.60	-24%	≤ 97%	≤ ±4%	≤ 10
250.8, ≥20s	250.84	91.97	1.40	-37.50	-0.01	1.40	-36%	≤ 93%	≤ ±4%	≤ 10
254.4, ≥20s	254.42	82.14	0.80	-48.99	-0.01	0.80	-48%	≤ 84%	≤ ±4%	≤ 10
258.0, ≥20s	258.02	36.49	1.00	-59.11	0.01	1.20	-60%	≤ 43%	≤ ±4%	≤ 10
254.4, ≥20s	254.44	80.50	1.40	-49.17	-0.01	1.40	-48%	≤ 84%	≤ ±4%	≤ 10
250.8, ≥20s	250.81	91.20	1.00	-37.84	-0.02	1.20	-36%	≤ 93%	≤ ±4%	≤ 10
247.2, ≥20s	247.22	96.22	0.80	-26.13	-0.02	1.00	-24%	≤ 97%	≤ ±4%	≤ 10
243.6, ≥20s	243.63	98.98	0.80	-13.84	-0.02	1.00	-12%	≤ 99%	≤ ±4%	≤ 10
240, ≥20s	240.02	99.98	1.80	1.96	0.02	2.40	0%	≤ 100%	≤ ±4%	≤ 10
220, ≥20s	220.10	99.99	0.80	1.95	0.02	0.80	0%	≤ 100%	≤ ±4%	≤ 10
217.4, ≥20s	217.39	99.60	2.00	8.70	0.00	4.20	9%	≤ 100%	≤ ±4%	≤ 10
214.8, ≥20s	214.81	97.85	2.60	19.30	0.01	4.20	18%	≤ 98%	≤ ±4%	≤ 10
212.2, ≥20s	212.21	95.15	2.20	27.42	0.01	4.00	26%	≤ 96%	≤ ±4%	≤ 10
209.6, ≥20s	209.60	93.18	1.60	33.93	-0.01	2.60	35%	≤ 94%	≤ ±4%	≤ 10
207, ≥20s	207.03	89.46	1.00	43.84	0.00	3.00	44%	≤ 90%	≤ ±4%	≤ 10
209.6, ≥20s	209.60	93.31	1.20	34.40	-0.01	2.80	35%	≤ 94%	≤ ±4%	≤ 10
212.2, ≥20s	212.2	95.92	1.20	24.91	-0.01	2.60	26%	≤ 96%	≤ ±4%	≤ 10

	2									
214.8, ≥20s	214.80	97.09	1.00	17.41	-0.01	2.00	18%	≤ 98%	≤ ±4%	≤ 10
217.4, ≥20s	217.41	99.79	2.60	7.82	-0.01	5.60	9%	≤ 100%	≤ ±4%	≤ 10
220, ≥20s	220.13	99.93	2.00	1.89	0.02	4.40	0%	≤ 100%	≤ ±4%	≤ 10
259, ≥20s	259.06	23.87	2.40	-60.95	-0.01	4.80	-60%	≤ 31%	≤ ±4%	≤ 10

Following configuration shall be inspected

Australia A	Available / ~~Not available~~		Australia B	Available / ~~Not available~~	
Australia C	Available / ~~Not available~~		New Zealand	Available / ~~Not available~~	
P(U) Configurable range	Points		Vw1		Vw2
	U [V]		235-255		240-265
	P/Sn		100%		0-20%
Q(U) Configurable range	Points		Vv1	Vv2	Vv3	Vv4
	U [V]		180-230	180-230	230-265	230-265
	P/Sn		30-60%	0%	0%	-30--60%

Note(s):
Active power is limited due to reactive power priority and current output limitation.

Plotting

Appendix G.2.2	TABLE: Combined volt-var and volt-watt response modes (enable by default)									P
Model AF1K-SL-1										

P(U) curve settings: Australia A	Points		Vw1			Vw2				
	U [V]		253			260				
	P/Sn		100%			20%				

Q(U) curve settings: Australia A	Points	Vv1		Vv2		Vv3		Vv4	
	U [V]	207		220		240		258	
	Q/Sn	44%		0%		0%		-60%	

Q(U) function (priority)	Enabled
P(U) function	Enabled

Test Conditions	Measurements						Target	Limits		
U [V]	U [V]	P/Sn [%]	$T_{settling}$ [s]	Q/Sn [%]	$\Delta Q/Sn$ [%]	$T_{settling}$ [s]	Q/Sn	P / Sn	$\Delta Q / Sn$	$T_{settling}$ [s]
230, ≥20s	230.01	100.00	1.00	2.40	0.02	1.80	0%	100%± 5%	--	--
240, ≥20s	240.03	99.99	0.80	2.33	0.02	1.00	0%	≤ 100%	≤ ±4%	≤ 10
243.6, ≥20s	243.62	98.61	1.40	-13.89	-0.02	3.00	-12%	≤ 99%	≤ ±4%	≤ 10
247.2, ≥20s	247.21	96.84	2.40	-25.69	-0.02	2.40	-24%	≤ 97%	≤ ±4%	≤ 10
250.8, ≥20s	250.84	92.65	1.00	-37.58	-0.02	2.00	-36%	≤ 93%	≤ ±4%	≤ 10
254.4, ≥20s	254.41	83.37	1.40	-49.17	-0.01	2.80	-48%	≤ 84%	≤ ±4%	≤ 10
258.0, ≥20s	258.02	37.28	1.00	-60.60	-0.01	2.20	-60%	≤ 43%	≤ ±4%	≤ 10
254.4, ≥20s	254.42	83.41	2.00	-49.34	-0.01	2.00	-48%	≤ 84%	≤ ±4%	≤ 10
250.8, ≥20s	250.82	92.35	2.00	-37.84	-0.02	2.20	-36%	≤ 93%	≤ ±4%	≤ 10
247.2, ≥20s	247.21	96.91	3.00	-26.06	-0.02	3.20	-24%	≤ 97%	≤ ±4%	≤ 10
243.6, ≥20s	243.63	98.44	3.00	-13.19	-0.01	3.00	-12%	≤ 99%	≤ ±4%	≤ 10
240, ≥20s	240.10	99.95	3.00	2.28	0.02	4.00	0%	≤ 100%	≤ ±4%	≤ 10
220, ≥20s	220.08	99.98	1.20	2.27	0.02	1.20	0%	≤ 100%	≤ ±4%	≤ 10
217.4, ≥20s	217.42	99.66	1.00	9.41	0.00	3.00	9%	≤ 100%	≤ ±4%	≤ 10
214.8, ≥20s	214.80	97.42	1.40	18.71	0.01	2.00	18%	≤ 98%	≤ ±4%	≤ 10
212.2, ≥20s	212.24	95.38	2.00	24.79	-0.01	2.40	26%	≤ 96%	≤ ±4%	≤ 10
209.6, ≥20s	209.62	93.55	4.00	34.36	-0.01	3.00	35%	≤ 94%	≤ ±4%	≤ 10
207, ≥20s	207.02	89.64	1.60	44.16	0.00	2.40	44%	≤ 90%	≤ ±4%	≤ 10
209.6, ≥20s	209.63	93.55	3.60	34.69	0.00	3.40	35%	≤ 94%	≤ ±4%	≤ 10
212.2, ≥20s	212.23	95.44	2.40	25.08	-0.01	2.80	26%	≤ 96%	≤ ±4%	≤ 10

214.8, ≥20s	214.82	96.83	2.80	17.42	-0.01	3.00	18%	≤ 98%	≤ ±4%	≤ 10
217.4, ≥20s	217.40	98.51	2.80	9.12	0.00	3.00	9%	≤ 100%	≤ ±4%	≤ 10
220, ≥20s	220.12	99.79	1.60	2.14	0.02	2.80	0%	≤ 100%	≤ ±4%	≤ 10
259, ≥20s	259.01	24.35	3.00	-59.20	0.01	4.00	-60%	≤ 31%	≤ ±4%	≤ 10

Following configuration shall be inspected					
Australia A	Available / ~~Not available~~		Australia B	Available / ~~Not available~~	
Australia C	Available / ~~Not available~~		New Zealand	Available / ~~Not available~~	
P(U) Configurable range	Points		Vw1		Vw2
	U [V]		235-255		240-265
	P/Sn		100%		0-20%
Q(U) Configurable range	Points	Vv1	Vv2	Vv3	Vv4
	U [V]	180-230	180-230	230-265	230-265
	P/Sn	30-60%	0%	0%	-30--60%

Note(s):
Active power is limited due to reactive power priority and current output limitation.

Plotting

Appendix G.2.3	TABLE: Volt-watt mode for charging of multiple mode inverters with energy storage									P

P(U) curve settings: Australia A	Points		Vw1-ch				Vw2-ch			
	U [V]		207				215			
	P_{charge}/ $P_{rated-ch}$		-20%				-100%			

Q(U) curve settings: Australia A	Points		Vv1		Vv2		Vv3		Vv4	
	U [V]		207		220		240		258	
	Q/Sn		44%		0%		0%		-60%	

Q(U) function (priority)	Enabled
P(U) function	Enabled

Test Conditions	Measurements						Target	Limits		
U [V]	U [V]	P_{charge}/ $P_{rated-ch}$ [%]	$T_{settling}$ [s]	Q/Sn	ΔQ/ Sn	$T_{settling}$ [s]	Q/Sn	P_{charge}/ $P_{rated-ch}$	ΔQ / Sn	$T_{settling}$ [s]
230, ≥20s	230.1	-99.95	0.2	2.22	--	0.2	--	-100%	--	--
215, ≥20s	215.1	-98.86	1.4	17.09	0.09	3.2	17%	≥ -99%	≤ ±4%	≤ 10
213, ≥20s	213.0	-78.53	0.8	22.80	-1.20	1.2	24%	≥ -80%	≤ ±4%	≤ 10
211, ≥20s	211.1	-57.43	1.6	29.45	-0.55	3.0	30%	≥ -60%	≤ ±4%	≤ 10
209, ≥20s	209.0	-37.05	1.0	36.71	-0.29	2.8	37%	≥ -40%	≤ ±4%	≤ 10
207, ≥20s	207.1	-16.40	1.0	43.39	-0.61	1.2	44%	≥ -20%	≤ ±4%	≤ 10
209, ≥20s	209.1	-36.67	1.4	36.72	-0.28	2.0	37%	≥ -40%	≤ ±4%	≤ 10
211, ≥20s	211.1	-57.10	2.0	29.92	-0.08	2.8	30%	≥ -60%	≤ ±4%	≤ 10
213, ≥20s	213.1	-76.83	4.0	22.86	-1.14	3.4	24%	≥ -80%	≤ ±4%	≤ 10
215, ≥20s	215.1	-98.71	1.2	16.12	-0.88	3.8	17%	≥ -99%	≤ ±4%	≤ 10
206, ≥20s	206.0	-16.23	1.6	44.00	0.00	4.5	44%	≥ -20%	≤ ±4%	≤ 10

Following configuration shall be inspected					
Australia B	Available / Not available		Australia B		Available / Not available
Australia C	Available / Not available		New Zealand		Available / Not available

P(U) Configurable range	Points		Vw1-ch		Vw2-ch	
	U [V]		180-230		240-265	
	P_{charge}/ $P_{rated-ch}$		0--20%		-100%	

Q(U) Configurable range	Points	Vv1	Vv2	Vv3	Vv4
	U [V]	180-230	180-230	230-265	230-265
	Q/Sn	30-60%	0%	0%	30--60%

Note(s):
$P_{rated-ch}$= 4.8 kW

Plotting

P/Sn[%]

60

40

20

0

-20

-40

-60

-80

-100

-120

206   207.1   209   209.1   211.1   211.1   213   213.1   215.1   215.1   230.1

Voltage[V]

P/Sn   Q/Sn   Limits_P/Sn   Limits(-)_Q/Sn   Limits(+)_Q/Sn

Appendix G.2.3	TABLE: Volt-watt mode for charging of multiple mode inverters with energy storage									P
Model	AF1K-SL-1									

P(U) curve settings: Australia A	Points			Vw1-ch				Vw2-ch		
	U [V]			207				215		
	P_{charge}/ $P_{rated-ch}$			-20%				-100%		

Q(U) curve settings: Australia A	Points		Vv1		Vv2		Vv3		Vv4	
	U [V]		207		220		240		258	
	Q/Sn		44%		0%		0%		-60%	

Q(U) function (priority)		Enabled								
P(U) function		Enabled								

Test Conditions	Measurements						Target	Limits		
U [V]	U [V]	P_{charge}/ $P_{rated-ch}$ [%]	$T_{settling}$ [s]	Q/Sn [%]	ΔQ/ Sn [%]	$T_{settling}$ [s]	Q/Sn	P_{charge}/ $P_{rated-ch}$	ΔQ / Sn	$T_{settling}$ [s]
230, ≥20s	230.1	-99.79	0.6	2.25	--	0.6	--	-100%	--	--
215, ≥20s	215.1	-98.92	1.0	15.86	-1.14	3.6	17%	≥ -99%	≤ ±4%	≤ 10
213, ≥20s	213.0	-77.98	3.0	23.07	-0.93	2.8	24%	≥ -80%	≤ ±4%	≤ 10
211, ≥20s	211.0	-56.95	1.0	29.81	-0.19	2.4	30%	≥ -60%	≤ ±4%	≤ 10
209, ≥20s	209.0	-36.14	1.2	37.12	0.12	3.6	37%	≥ -40%	≤ ±4%	≤ 10
207, ≥20s	207.0	-16.53	1.6	43.90	-0.10	3.0	44%	≥ -20%	≤ ±4%	≤ 10
209, ≥20s	209.0	-35.86	1.2	37.18	0.18	3.0	37%	≥ -40%	≤ ±4%	≤ 10
211, ≥20s	211.1	-56.58	1.0	30.32	0.32	2.8	30%	≥ -60%	≤ ±4%	≤ 10
213, ≥20s	213.0	-77.18	2.0	23.17	-0.83	2.4	24%	≥ -80%	≤ ±4%	≤ 10
215, ≥20s	215.1	-98.59	2.4	16.24	-0.76	3.6	17%	≥ -99%	≤ ±4%	≤ 10
206, ≥20s	206.0	-16.10	1.0	43.95	-0.05	4.2	44%	≥ -20%	≤ ±4%	≤ 10

Following configuration shall be inspected										
Australia B		Available / Not available			Australia B			Available / Not available		
Australia C		Available / Not available			New Zealand			Available / Not available		

P(U) Configurable range	Points			Vw1-ch				Vw2-ch		
	U [V]			180-230				240-265		
	P_{charge}/ $P_{rated-ch}$			0--20%				-100%		

Q(U) Configurable range	Points		Vv1		Vv2		Vv3		Vv4	
	U [V]		180-230		180-230		230-265		230-265	
	Q/Sn		30-60%		0%		0%		30--60%	

Note(s): $P_{rated-ch}$ =1kW										
Plotting										

Appendix H	TABLE: Active anti-islanding test							P

The method used to provide active anti-islanding protection:	☒ Frequency shift ☐ Frequency instability ☐ Power variation ☐ Current injection ☐ Other: _____

EUT type:	☒ Single PV inverter ☐ Single-phase combination, number of inverters under test_____ ☐ Single-phase inverters used in three phase combinations, number of inverters under test_____

☒ Test according the IEC 62116: 2014 (Without reactive power output)

No.	PEUT[1] (% of EUT rating)	Reactive load (% of QL in 6.1.d)1)	PAC [2] (% of nominal)	QAC [3] (% of nominal)	Run on time (ms)	P_{EUT} (W)	Actual Qf	Remarks [4]
1.	100	100	0	0	322	6000	0.99	Test A at BL
2.	66	66	0	0	300	3960	1.00	Test B at BL
3.	33	33	0	0	281	1980	0.98	Test C at BL
4.	100	100	-5	-5	304	6000	1.01	Test A at IB
5.	100	100	-5	0	289	6000	1.04	Test A at IB
6.	100	100	-5	+5	212	6000	1.07	Test A at IB
7.	100	100	0	-5	277	6000	0.96	Test A at IB
8.	100	100	0	+5	237	6000	1.01	Test A at IB
9.	100	100	+5	-5	210	6000	0.92	Test A at IB
10.	100	100	+5	0	280	6000	0.94	Test A at IB
11.	100	100	+5	+5	282	6000	0.96	Test A at IB
12.	66	66	0	-5	222	3960	0.97	Test B at IB
13.	66	66	0	-4	228	3960	0.98	Test B at IB
14.	66	66	0	-3	230	3960	0.98	Test B at IB
15.	66	66	0	-2	280	3960	0.99	Test B at IB
16.	66	66	0	-1	236	3960	0.99	Test B at IB
17.	66	66	0	1	238	3960	1.00	Test B at IB
18.	66	66	0	2	256	3960	1.01	Test B at IB
19.	66	66	0	3	254	3960	1.01	Test B at IB
20.	66	66	0	4	242	3960	1.02	Test B at IB
21.	66	66	0	5	168	3960	1.02	Test C at IB
22.	33	33	0	-5	203	1980	0.96	Test C at IB
23.	33	33	0	-4	218	1980	0.96	Test C at IB
24.	33	33	0	-3	220	1980	0.97	Test C at IB
25.	33	33	0	-2	242	1980	0.97	Test C at IB
26.	33	33	0	-1	230	1980	0.98	Test C at IB
27.	33	33	0	1	263	1980	0.99	Test C at IB
28.	33	33	0	2	245	1980	0.99	Test C at IB
29.	33	33	0	3	256	1980	1.00	Test C at IB
30.	33	33	0	4	200	1980	1.00	Test C at IB
31.	33	33	0	5	160	1980	1.01	Test C at IB

Remark:

1) PEUT: EUT output power

2) PAC: Real power flow at S1 in Figure 1. Positive means power from EUT to utility. Nominal is the 0 % test condition value.

3) QAC: Reactive power flow at S1 in Figure 1. Positive means power from EUT to utility. Nominal is the 0 % test condition value.

4) BL: Balance condition, IB: Imbalance condition.

Tek PreVu   M 1.00 s

Zoom Factor: 10 X   Zoom Position: 87.0ms

		a	−84.00ms	−13.75mA
		b	238.0ms	70.31mA
		△	△322.0ms	△84.06mA

| 1 | 1.00 A | | Z 100ms | 500kS/s | 1 | ∫ |
| 3 | 50.0 A | 4 | 500 V | 5M points | | 0.00 A |

	Value	Mean	Min	Max	Std Dev
RMS	73.12mA	73.12m	73.12m	73.12m	0.000

$P_{EUT}100\%, P_{AC}0\%, Q_{AC}0\%, = 322ms$

Tek PreVu   M 1.00 s

Zoom Factor: 10 X   Zoom Position: −59.0ms

		a	−178.0ms	67.81mA
		b	122.0ms	64.22mA
		△	△300.0ms	△3.594mA

| 1 | 1.00 A | | Z 100ms | 500kS/s | 1 | ∫ |
| 3 | 50.0 A | 4 | 500 V | 5M points | | 0.00 A |

	Value	Mean	Min	Max	Std Dev
RMS	67.18mA	67.18m	67.18m	67.18m	0.000

$P_{EUT}66\%, P_{AC}0\%, Q_{AC}0\%, = 300ms$

Tek PreVu   M 1.00 s

Zoom Factor: 10 X   Zoom Position: 97.0ms

		a	−124.0ms	54.38mA
		b	157.0ms	74.22mA
		△	△281.0ms	△19.84mA

| 1 | 1.00 A | | Z 100ms | 500kS/s | 1 | ∫ |
| 3 | 20.0 A | 4 | 500 V | 5M points | | 0.00 A |

	Value	Mean	Min	Max	Std Dev
RMS	69.26mA	69.26m	69.26m	69.26m	0.000

$P_{EUT}33\%, P_{AC}0\%, Q_{AC}0\%, = 281ms$

Appendix I.2.2	TABLE: Overvoltage 2 (V>>) test					P
Step	Condition	Time	Measurement			Limitation [ms]
			Trip time [ms]			
			L1	L2	L3	
a), b), c), d)	100%Sn /230Vac, 262.5Vac ->277.5Vac	400ms	120	--	--	≤200
			120	--	--	
			120	--	--	
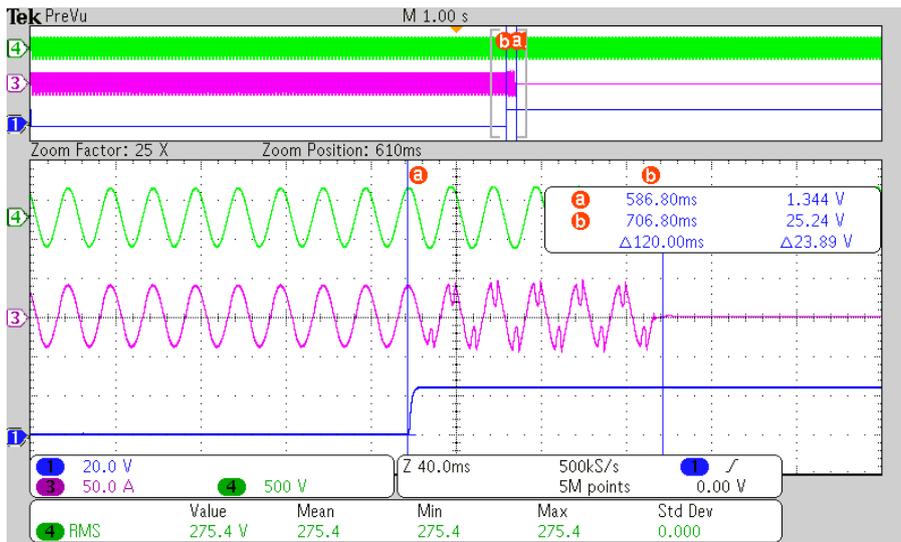
Condition	Setting [V]	Measurement			Limitation [V]
		Trip value [V]			
		L1	L2	L3	
U>>	275	275.4	--	--	±2.3
		275.4	--	--	
		275.3	--	--	

	Voltage	Measurement			Limitation	
e)		Delay time	Power Gradient	P/Pn	Delay time	Power Gradient
	230Vac	62 s	16.22%Pn/min	50.1%	≥60s	16.67%Pn/min
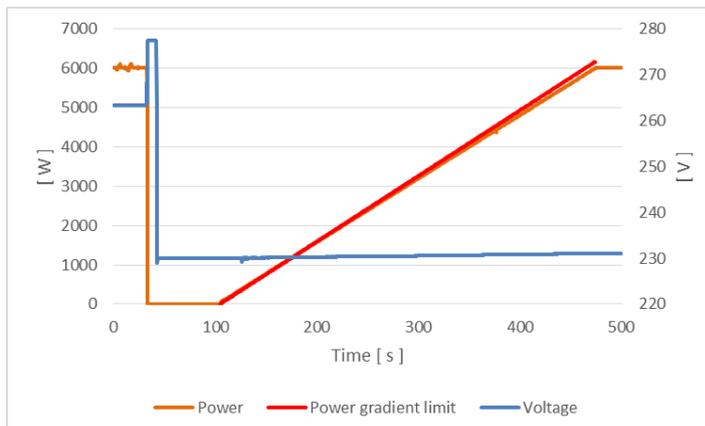
Note:

Step the grid source voltage from 262.5Vac to 277.5Vac with the voltage step completed within 2 ms and **occurring at the zero crossing**. Record the time interval between the start of the voltage step and the device under test disconnecting from the grid source.

Appendix I.2.3			TABLE: Undervoltage 2 (V<<) test			P
Step	Condition	Time	Measurement			Limitation
			Trip time [s]			
			L1	L2	L3	
a)	50%Sn, 230Vac->67.5Vac	5 s	1.55	-	-	1 s to 2 s
			1.56	-	-	
			1.55	-	-	
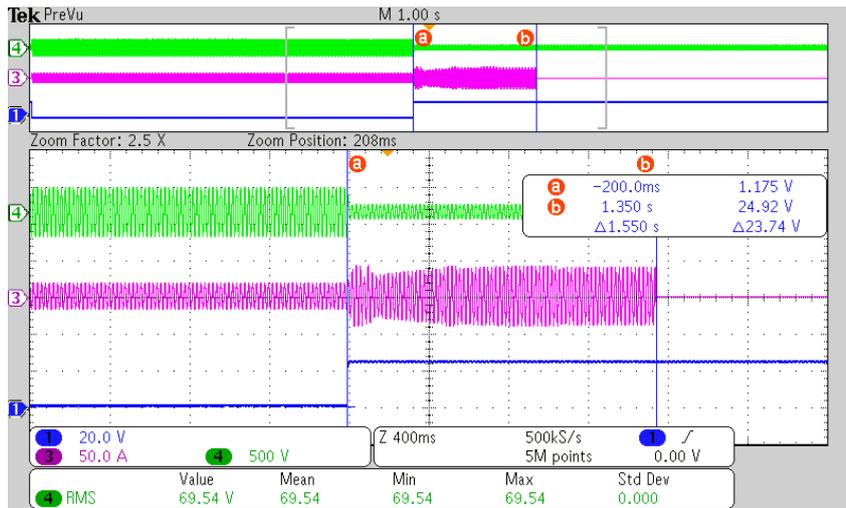
Note:
Step the grid source voltage from 230Vac to 67.5Vac with the voltage step completed within 2 ms and **occurring at the zero crossing**.

Condition	Setting [V]	Measurement			Limitation [V]
		Trip value [V]			
		L1	L2	L3	
U<<	70	69.54	--	--	±2.3
		69.44	--	--	
		69.54	--	--	

	Voltage	Measurement			Limitation	
		Delay time	Power Gradient	P/Pn	Delay time	Power Gradient
b)	230 Vac	62 s	16.13%Pn/min	50.1%	≥60s	16.67%Pn/min
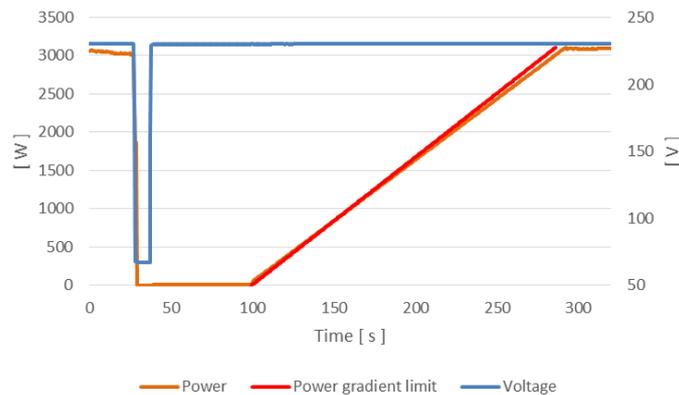
c)	Voltage	Time	Measurement				Limitation
			Time [ms]				
			All	L1	L2	L3	
	50Vac	900ms	900	--	--	--	No disconnection
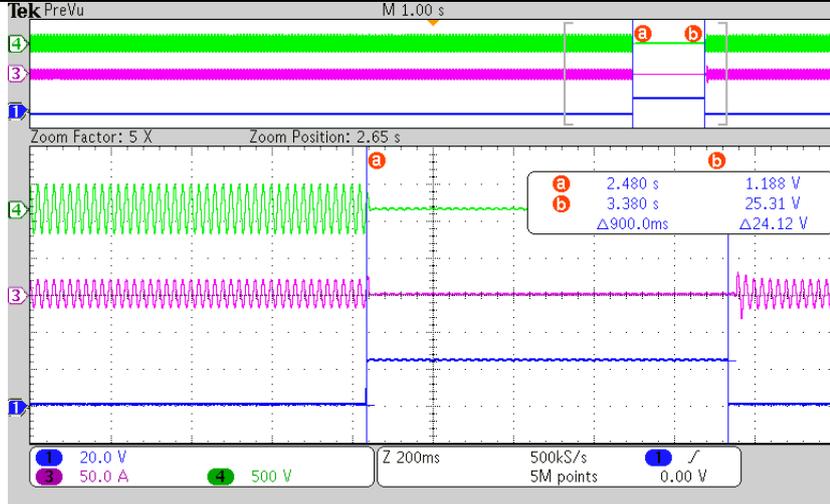
Note:
Step the grid source voltage from 230Vac to 50Vac with the voltage step completed within 2 ms and **occurring at the zero crossing**.

d)	Voltage	Time	Measurement	Limitation
			P/Pn	
	230Vac	400ms	50.15%	(50% ±4%) Pn

Appendix I.2.4			TABLE: Undervoltage 1 (V<) test			P
Step	Condition	Time	Measurement			Limitation
			Trip time [s]			
			L1	L2	L3	
a), b)	50%Sn /230Vac, 182.5Vac-> 178Vac	15s	10.50	--	--	10s to 11s
			10.58	--	--	
			10.50	--	--	

	Condition	Setting [V]	Measurement			Limitation [V]
			Trip value [V]			
c)			L1	L2	L3	
	U<	180	178.6	--	--	±2.3
			178.7	--	--	
			178.7	--	--	

Note:
Step the grid source voltage from 182.5Vac to 178Vac, dwell time 15s.

--	Voltage	Time	Measurement			Limitation	
			Delay time	Power Gradient	P/Pn	Delay time	Power Gradient
d)	203Vac	120s	No reconnection			Not reconnection	
e)	207Vac	120s	61s	16.35%Pn/ min	50.1%	≥60s	16.67%Pn/mi n
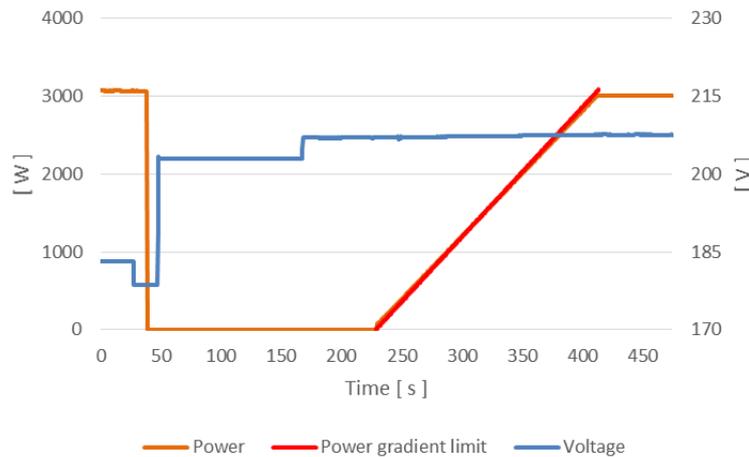
Note:

Appendix I.2.5		TABLE: Overvoltage 1 (V>) test				P
Step	Condition	Time	Measurement			Limitation
			Trip time [s]			
			L1	L2	L3	
a), b)	50%Sn / 230Vac, 262.5Vac-> 267Vac	5s	1.49	--	--	1s to 2s
			1.51	--	--	
			1.50	--	--	

Note:
Step the grid source voltage from 262.5Vac to 267Vac, dwell time 5s.

	Condition	Setting [V]	Measurement			Limitation [V]
			Trip value [V]			
c)			L1	L2	L3	
	U>	265	265.9	--	--	±2.3
			265.8	--	--	
			265.7	--	--	

--	Voltage	Time	Measurement			Limitation	
			Delay time	Power Gradient	P/Pn	Delay time	Power Gradient
d)	255Vac	120s	Not reconnection			Not reconnection	
e)	251Vac	120s	62s	16.3% Pn/min	50.1%	≥60s	16.67%Pn/min

Note:

| Appendix I.3	TABLE: Voltage disturbance withstand tests (Test 1)									P
	Condition					Measurement*				
Step	P/Sn [%]	Voltage-Phase L1 [Vac]	Voltage-Phase L2 [Vac]	Voltage-Phase L3 [Vac]	Time [s]	P/Sn [%]	Voltage-Phase L1 [Vac]	Voltage-Phase L2 [Vac]	Voltage-Phase L3 [Vac]	Time [s]
a), b)	50	230	230	230	3	50.33	230.3	--	--	3.00
c), d)	50	267.5	230	230	0.95	0.43	266.3	--	--	0.95
e), f)	50	230	230	230	2	50.10	230.4	--	--	2.00
g), h)	50	50	230	230	0.95	0.35	49.8	--	--	0.95
i), j)	50	150	230	230	8	1.16	149.5	--	--	8.00
k), l)	50	230	230	230	15	50.38	230.4	--	--	15.00
m), n)	50	50	230	230	0.5	0.35	49.9	--	--	0.50
o), p)	50	230	230	230	2	50.36	230.3	--	--	2.00
q), r)	50	100	230	230	4.5	0.80	99.4	--	--	4.50
s), n)	50	50	230	230	0.5	0.34	49.8	--	--	0.50
o), p)	50	230	230	230	2	50.36	230.3	--	--	2.00
q), r)	50	100	230	230	4.5	0.81	99.7	--	--	4.50
u), v)	50	230	230	230	3	49.60	230.3	--	--	3.00

Note:
*) The measurement value of 200ms after dip begin and 400ms after dip recovery were recorded.

All the grid test voltage with the step change shall complete within 2 ms and **occurring at the zero crossing** of the grid source voltage.

Graph: Test1

Appendix I.3	TABLE: Voltage disturbance withstand tests (Test 2)									P
	Condition					Measurement*				
Step	P/Sn [%]	Voltage-Phase L1 [Vac]	Voltage-Phase L2 [Vac]	Voltage-Phase L3 [Vac]	Time [s]	P/Sn [%]	Voltage-Phase L1 [Vac]	Voltage-Phase L2 [Vac]	Voltage-Phase L3 [Vac]	Time [s]
a), b)	50	230	230	230	3	50.30	230.3	--	--	3.00
c), d)	50	267.5	230	230	0.95	0.41	266.3	--	--	1.00
e), f)	50	230	230	230	2	50.25	230.4	--	--	2.00
g), h)	50	50	230	230	0.95	0.35	49.9	--	--	0.95
i), j)	50	150	230	230	8	1.18	149.5	--	--	8.00
k), l)	50	230	230	230	15	50.42	230.4	--	--	15.00
m), n)	50	50	230	230	0.5	0.75	50.0	--	--	0.50
o), p)	50	230	230	230	2	50.40	230.4	--	--	2.00
q), r)	50	100	230	230	4.5	0.80	99.6	--	--	4.50
s), n)	50	50	230	230	0.5	0.34	49.9	--	--	0.50
o), p)	50	230	230	230	2	50.00	230.3	--	--	2.00
q), r)	50	100	230	230	4.5	0.80	99.8	--	--	4.50
u), v)	50	230	230	230	3	49.15	230.3	--	--	3.00

Note:
*) The measurement value of 200ms after dip begin and 400ms after dip recovery were recorded.

All the grid test voltage with the step change shall complete within 2 ms and **occurring at the zero crossing** of the grid source voltage.

Graph: Test2
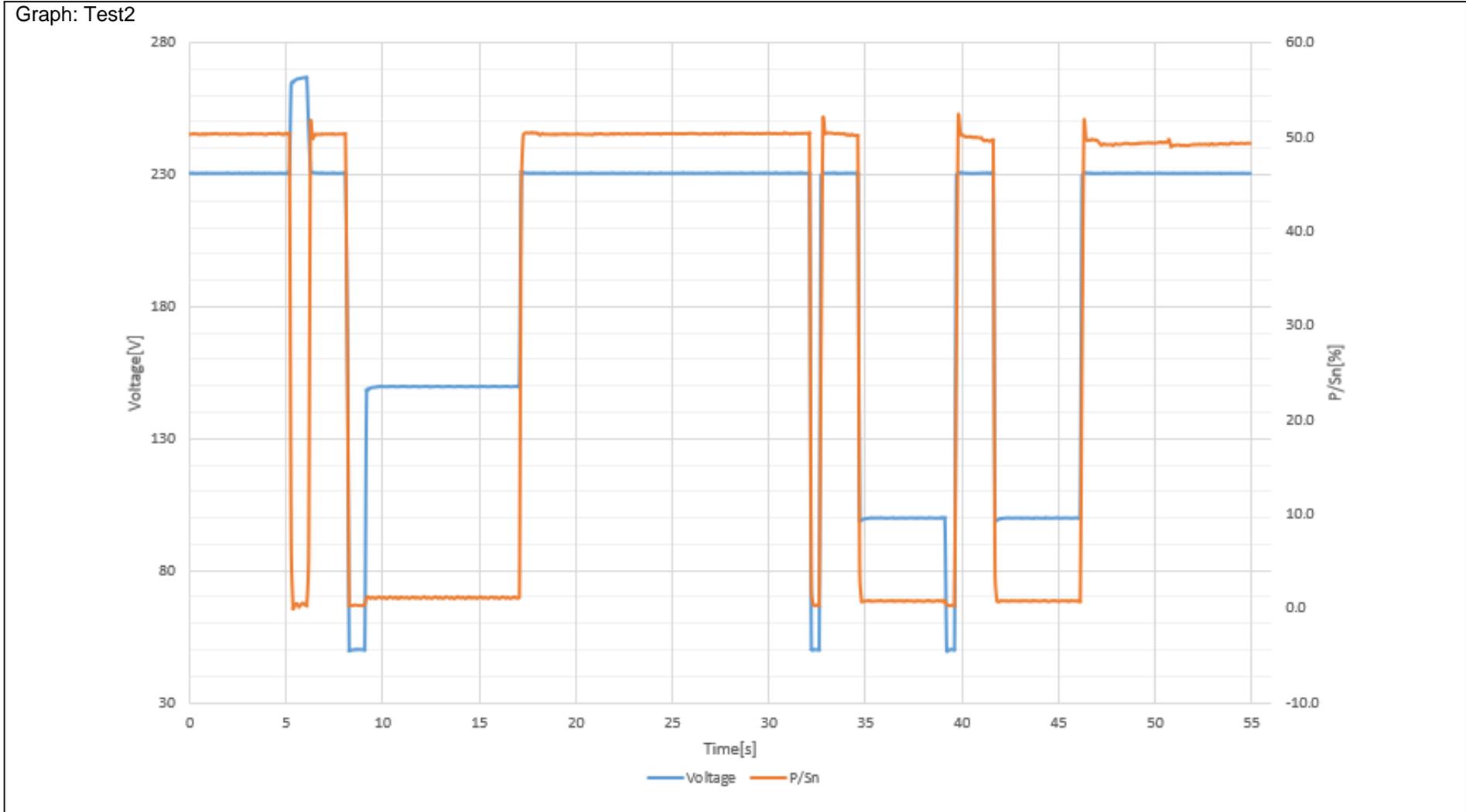
Appendix I.3	TABLE: Voltage disturbance withstand tests (Test 3)									P
Step	Condition					Measurement*				
	P/Sn [%]	Voltage-Phase L1 [Vac]	Voltage-Phase L2 [Vac]	Voltage-Phase L3 [Vac]	Time [s]	P/Sn [%]	Voltage-Phase L1 [Vac]	Voltage-Phase L2 [Vac]	Voltage-Phase L3 [Vac]	Time [s]
a), b)	50	230	230	230	3	50.36	230.3	--	--	3.00
c), d)	50	267.5	230	230	0.95	0.40	266.4	--	--	1.00
e), f)	50	230	230	230	2	50.26	230.4	--	--	2.00
g), h)	50	50	230	230	0.95	0.36	49.9	--	--	0.95
i), j)	50	150	230	230	8	1.16	149.6	--	--	8.00
k), l)	50	230	230	230	15	50.43	230.4	--	--	15.00
m), n)	50	50	230	230	0.5	0.36	49.9	--	--	0.50
o), p)	50	230	230	230	2	50.18	230.5	--	--	2.00
q), r)	50	100	230	230	4.5	0.80	99.6	--	--	4.50
s), n)	50	50	230	230	0.5	0.34	49.8	--	--	0.50
o), p)	50	230	230	230	2	49.65	230.3	--	--	2.00
q), r)	50	100	230	230	4.5	0.81	99.8	--	--	4.50
u), v)	50	230	230	230	3	48.72	230.3	--	--	3.00

Note:
*) The measurement value of 200ms after dip begin and 400ms after dip recovery were recorded.

All the grid test voltage with the step change shall complete within 2 ms and **occurring at the zero crossing** of the grid source voltage.

Graph: Test3
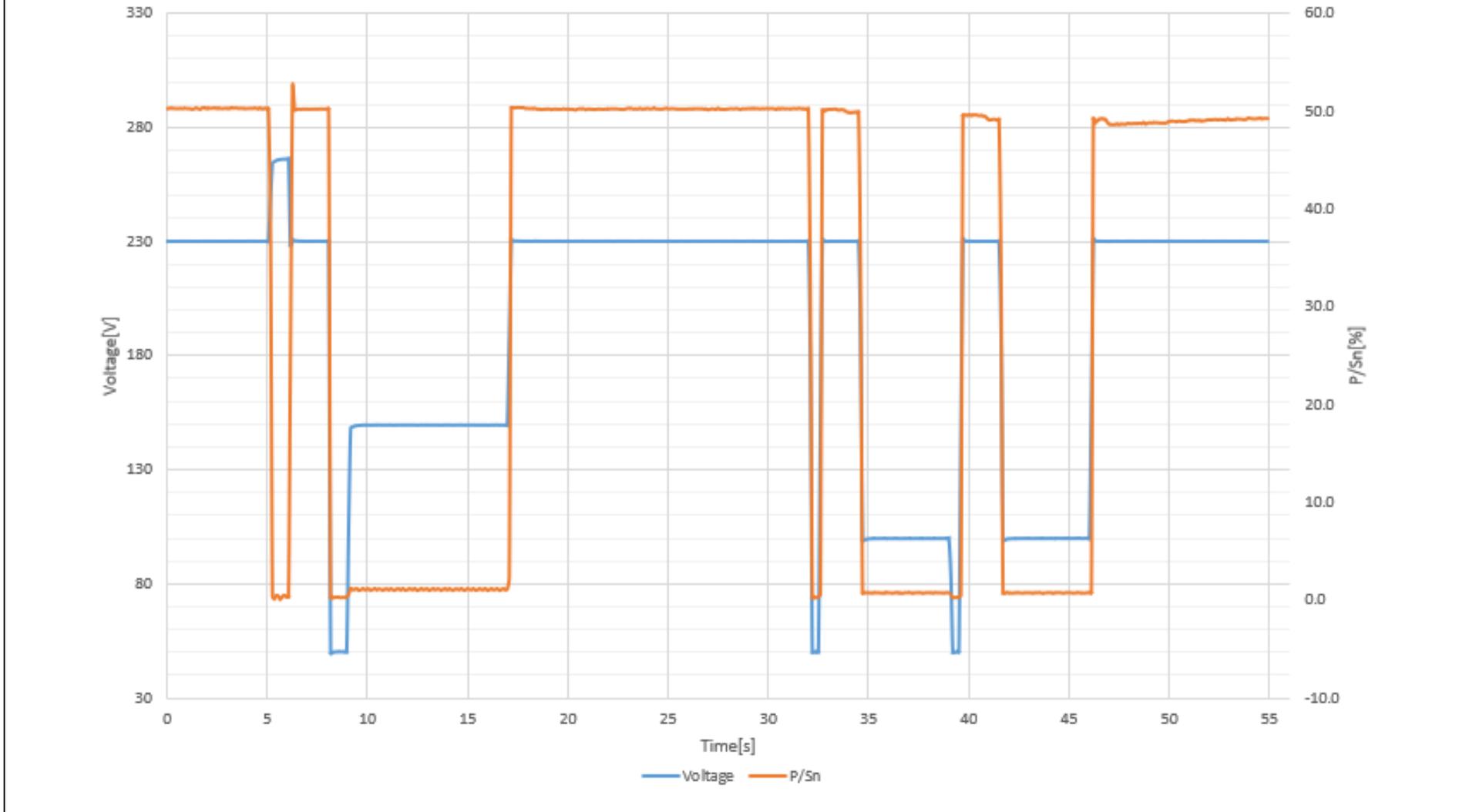
Appendix I.4.2	TABLE: Under-frequency 1 (F<) test					P
Step	Condition	Setting Australia A [Hz]	Measurement			Limitation [Hz]
			Trip value [Hz]			
a), b),	50%Sn /50Hz->UF1	47	46.99	46.99	46.99	±0.01

Note:
Slowly decrease the frequency of the grid source until the device under test disconnects from the grid source. Record the frequency at which disconnection occurs.

Step	Frequency [Hz]	Measurement	Limitation
		Delay time	Delay time
c)	50	61 s	≥60s

Step	Condition	Setting Australia A [ms]	Measurement			Limitation [ms]
			Trip time [ms]			
d)	UF1+0.1Hz->40Hz (4Hz/s)	1500	1537	1534	1541	1000-2000
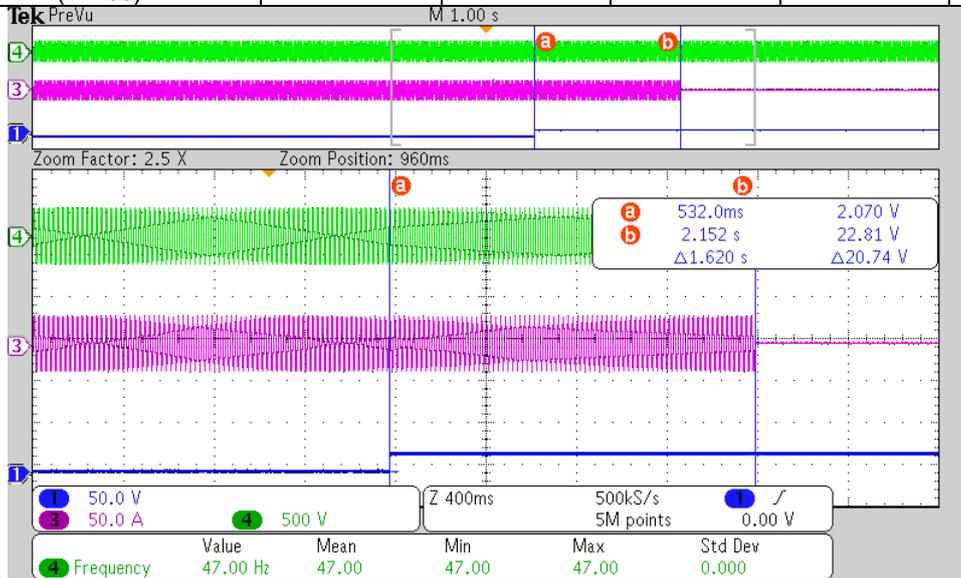
Step	Condition	Measurement	Limitation
		Delay time	Delay time
e)	47.4Hz, 2*T$_{delay\ time\ at\ c)}$	Not reconnection	Not reconnection
f)	48Hz	62 s	≥60s

Appendix I.4.3	TABLE: Over-frequency 1 (F>) test					P
Step	Condition	Setting Australia A [Hz]	Measurement			Limitation [Hz]
			Trip value [Hz]			
a), b),	50%Sn /50Hz->OF1	52	52.01	52.00	52.00	±0.01

Note:
Slowly decrease the frequency of the grid source until the device under test disconnects from the grid source. Record the frequency at which disconnection occurs.

Step	Frequency [Hz]	Measurement	Limitation
		Delay time	Delay time
c)	50	62 s	≥60s

Step	Condition	Setting Australia A [ms]	Measurement			Limitation [ms]
			Trip time [ms]			
d)	OF1-0.1Hz->60Hz (4Hz/s)	100	157	159	151	≤200

Step	Condition	Measurement	Limitation
		Delay time	Delay time
e)	50.2Hz, 2*T$_{delay\ time\ at\ c)}$	Not reconnection	Not reconnection
f)	50.1Hz	62 s	≥60s

Appendix I.5	TABLE: Voltage phase angle shift test						P
Test Condition		Duration [ms]	Measurement*			Limit	
			Test1	Test2	Test3		
			P / Sn [%]			--	P/Sn
All	The active power level after the device under test has been set to 50 ± 5 % of its rated current output [I.5.2 (b)]	--	50.88	51.00	50.92	--	--
L1	The active power level 400 ms after the relative angle of phase-a has been shifted by 60° ± 3° and been restored [I.5.2(e)]	500	50.80	50.88	50.87	No disconnect	46% to 54%
L2	The active power level 400 ms after the relative angle of phase-b has been shifted by 60° ± 3° and been restored [I.5.2(e)]	500	--	--	--	No disconnect	46% to 54%
L3	The active power level 400 ms after the relative angle of phase-c has been shifted by 60° ± 3° and been restored [I.5.2(e)]	500	--	--	--	No disconnect	46% to 54%
All	The active power level 400 ms after the voltage angles of all three phases have been shifted by 20° ± 3° and been restored [I.5.2(i)]	60000	--	--	--	No disconnect	46% to 54%
Note(s):							

Test1
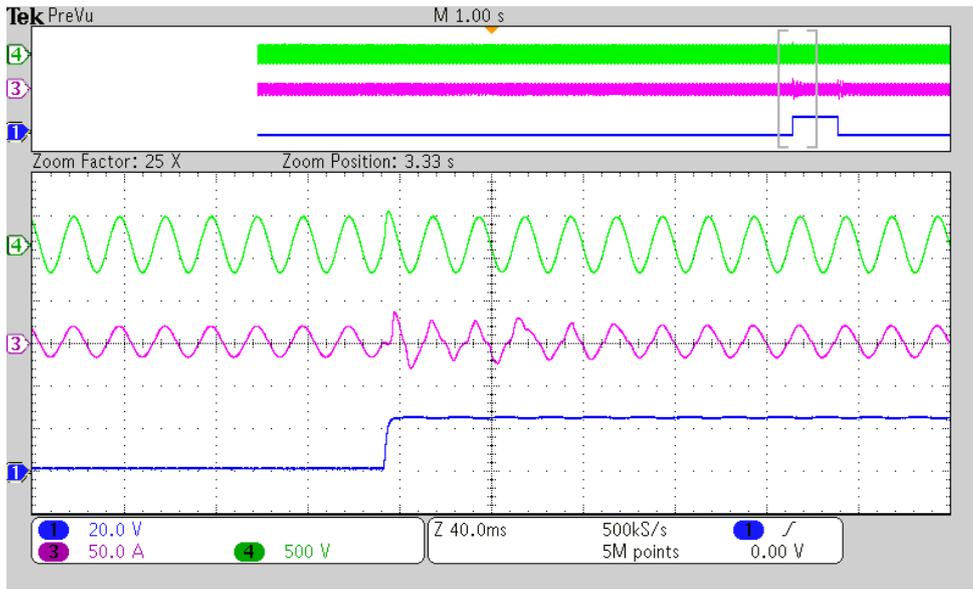
L1: Initial-> Initial+60°
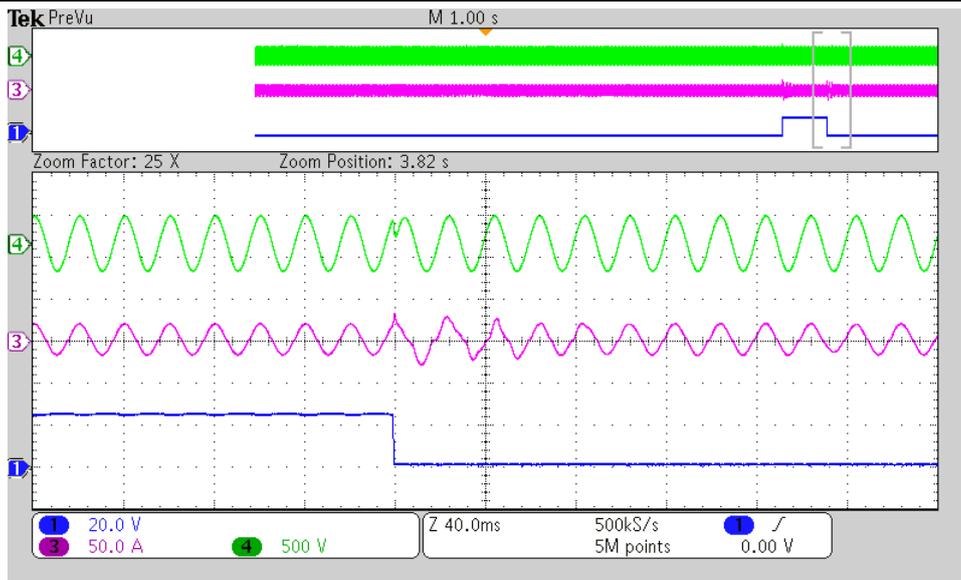
L1: Initial+60°->Initial

Test2
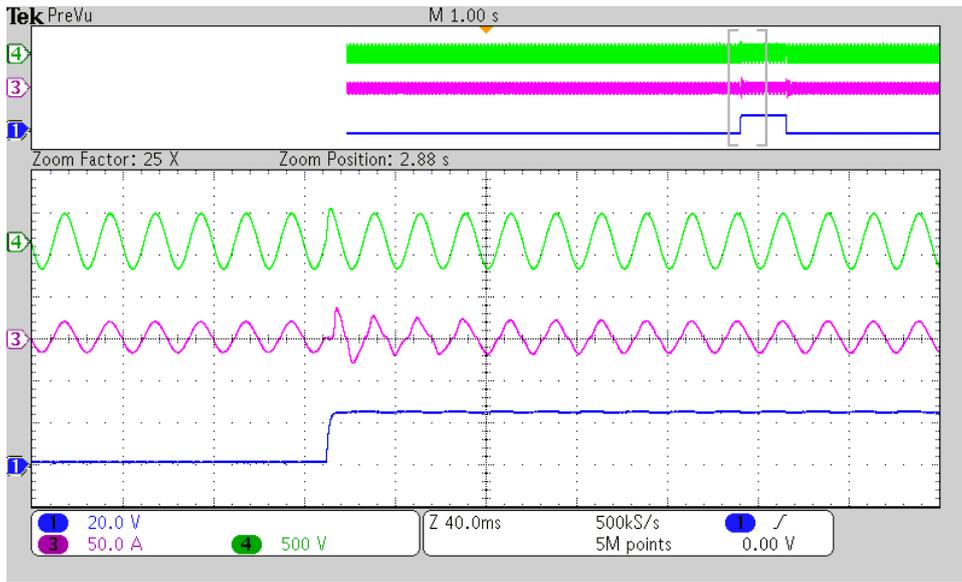
L1: Initial-> Initial+60°
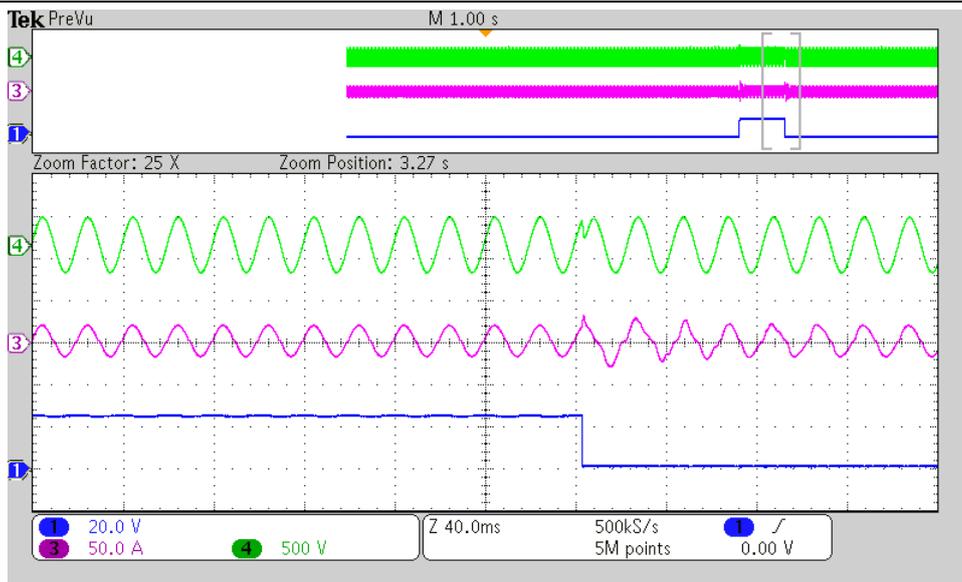
L1: Initial+60°->Initial

Test3
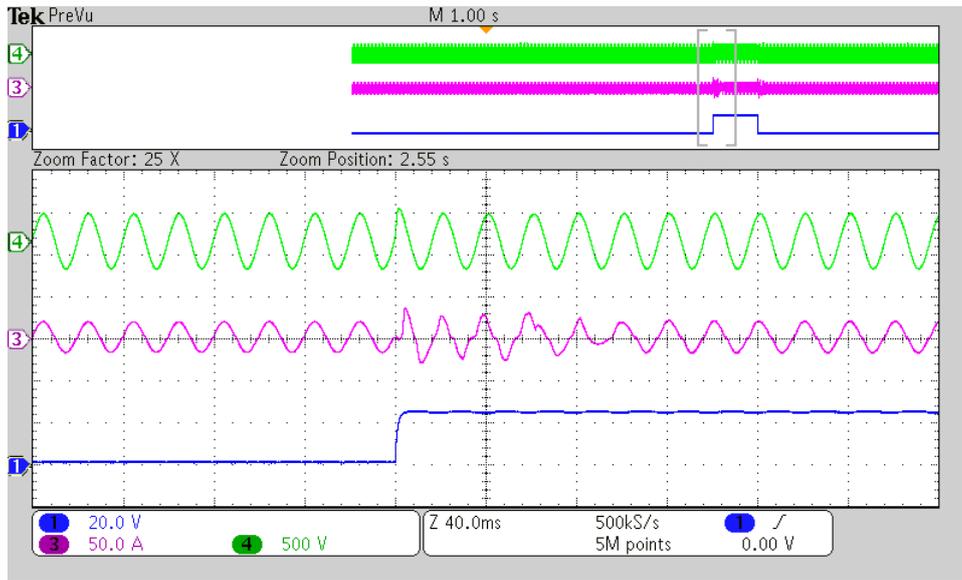
L1: Initial-> Initial+60°
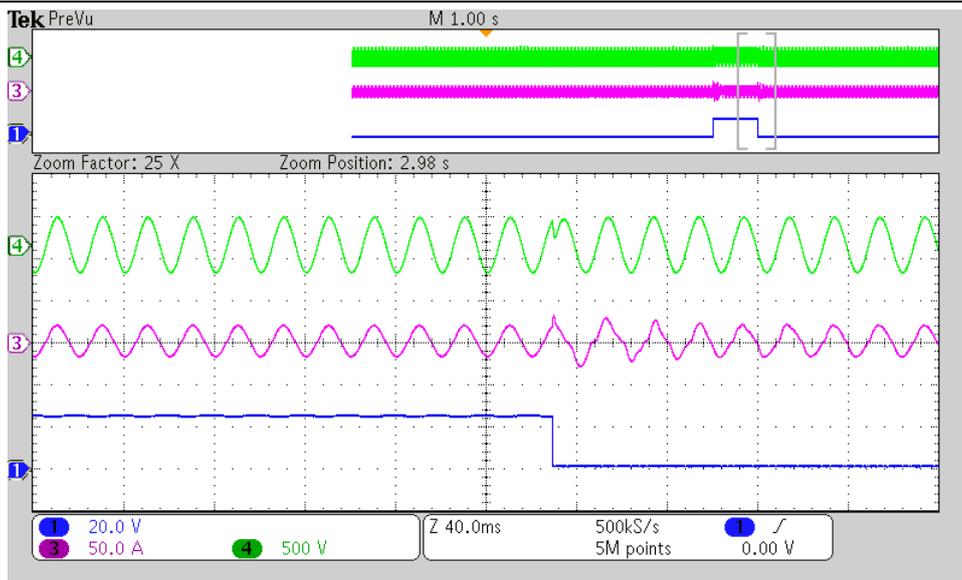
L1: Initial+60°->Initial

Appendix J.2	TABLE: Sustained for voltage variations					P

Table 4.3 — Settings for $V_{nom-max}$

Region	Default setpoint
Australia A	258 V
Australia B	258 V
Australia C	258 V
New Zealand	249 V
Allowable range	244 V to 258 V

Step	Condition	Setting Australia A [V]	Measurement		Limitation	
			Vnom-max [V]	Trip time [s]	Vnom-max [V]	Trip time [s]
a), b)	50%Sn, 230Vac, 10min.	258	--	--	≤ ±2.3	≤ 30
c)	257Vac, 5min.		--	--		
e)	259Vac, 10min.		258.04	--		
f)	230Vac, 10min.		--	--		
a), b)	50%Sn, 230Vac, 10min.		--	--		
c)	257Vac, 5min.		--	--		
e)	259Vac, 10min.		258.03	--		
f)	230Vac, 10min.		--	--		
a), b)	50%Sn, 230Vac, 10min.		--	--		
c)	257Vac, 5min.		--	--		
e)	259Vac, 10min.		258.02	--		
f)	230Vac, 10min.		--	--		
g)	258Vac, 10min.		--	--		
h)	259.5Vac		--	3.2		

Step	Condition	Measurement	Limitation
		Delay time	Delay time
i)	230Vac	61 s	≥60s

Appendix J.3.2	TABLE: Test for an increase in frequency for inverters without energy storage			P
LFSM-O curve settings: Australia A	Points	f_{ULCO}	$f_{trasition}$	f_{Pmin}
	Hz	50.25	--	52.0
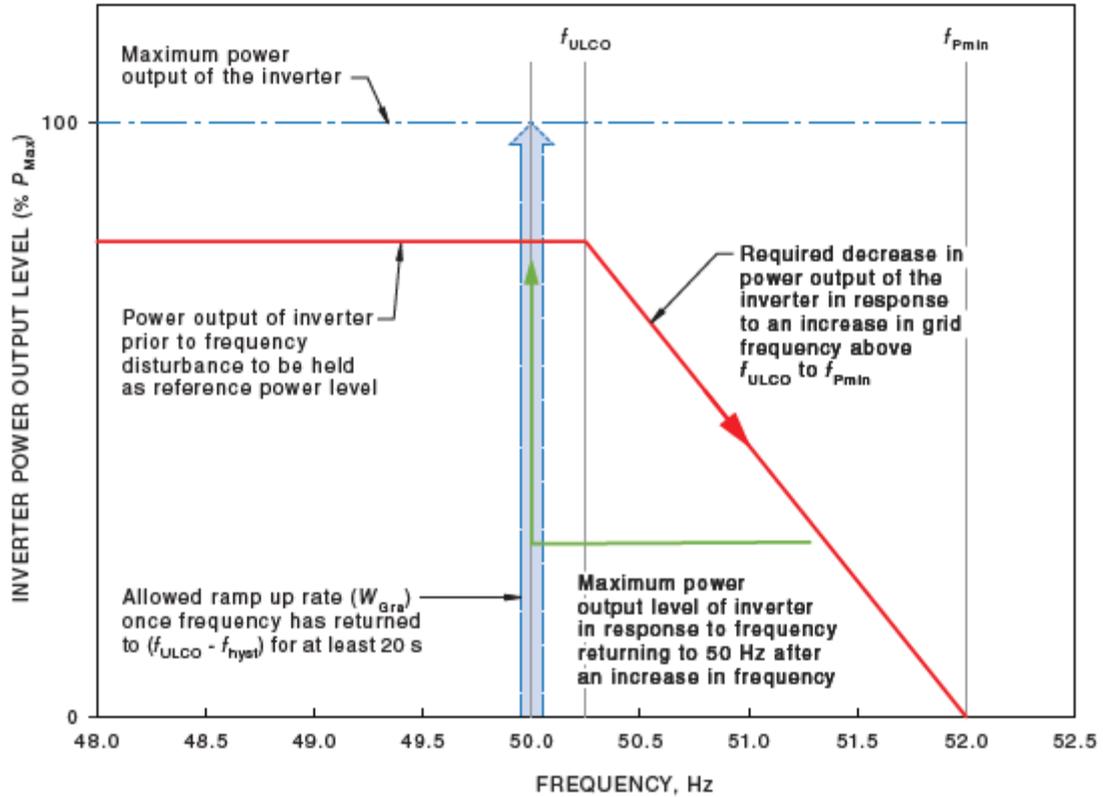
Figure 4.3 — Example frequency response for an increase in frequency for f_{Pmin} of 52 Hz

$$P_{out} = P_{ref}\left[1 - \frac{(f - f_{ULCO})}{(f_{Pmin} - f_{ULCO})}\right]$$

Test Conditions		Measurements			Target value	Δ	Limit		
f [Hz]	P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/Pn [%]	Δ P/Sn [%]	Δ P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]
50.0	50.38	--	--	--	50	0.38			
50.2	50.39	--	--	--	50	0.39			
50.4	47.90	0.4	7.5	--	46	1.90			
50.6	41.92	0.4	7	--	40	1.92			
50.8	36.19	0.4	5.5	--	34	2.19			
51.0	30.06	0.4	5	--	29	1.06			
51.2	24.30	0.4	5	--	23	1.30			
51.4	18.39	0.4	4.5	--	17	1.39	≤ ±4	≤ 1	≤ 10
51.6	12.34	0.4	4.5	--	11	1.34			
51.8	6.54	0.4	4	--	6	0.54			
51.6	6.51	--	--	--	6	0.51			
51.4	6.51	--	--	--	6	0.51			
51.2	6.52	--	--	--	6	0.52			
51.0	6.53	--	--	--	6	0.53			

50.8	6.53	--	--	--	6	0.53
50.6	6.53	--	--	--	6	0.53
50.4	6.53	--	--	--	6	0.53
50.2	6.54	--	--	--	6	0.54
50.0	50.40	--	--	15.48	50	0.40
Ramp to 51.0Hz with 4Hz/s	30.04	0.4	7	--	29	1.04
50.8	30.03	--	--	--	29	1.03
50.6	30.02	--	--	--	29	1.02
50.4	30.02	--	--	--	29	1.02
50.2	30.02	--	--	--	29	1.02
50.0	50.28	--	--	15.59	50	0.28

Following configuration shall be inspected

Australia A	Available / ~~Not available~~	Australia B	Available / ~~Not available~~
Australia C	Available / ~~Not available~~	New Zealand	Available / ~~Not available~~

LFSM-O Configurable range	Points	f_{ULCO}	$f_{trasition}$	f_{Pmin}
	Hz	50.1-50.5	50.5-52.0	51.0-53.0

Diagram

Graph of J.3.2 freq. and power level

P/Sn [%] vs Frequency [Hz]

Legend: ⋯⋯ Limit (+)   ━━ P/Sn   ⋯⋯ Limit (-)

Power change rate curve for J.3.2 step i)
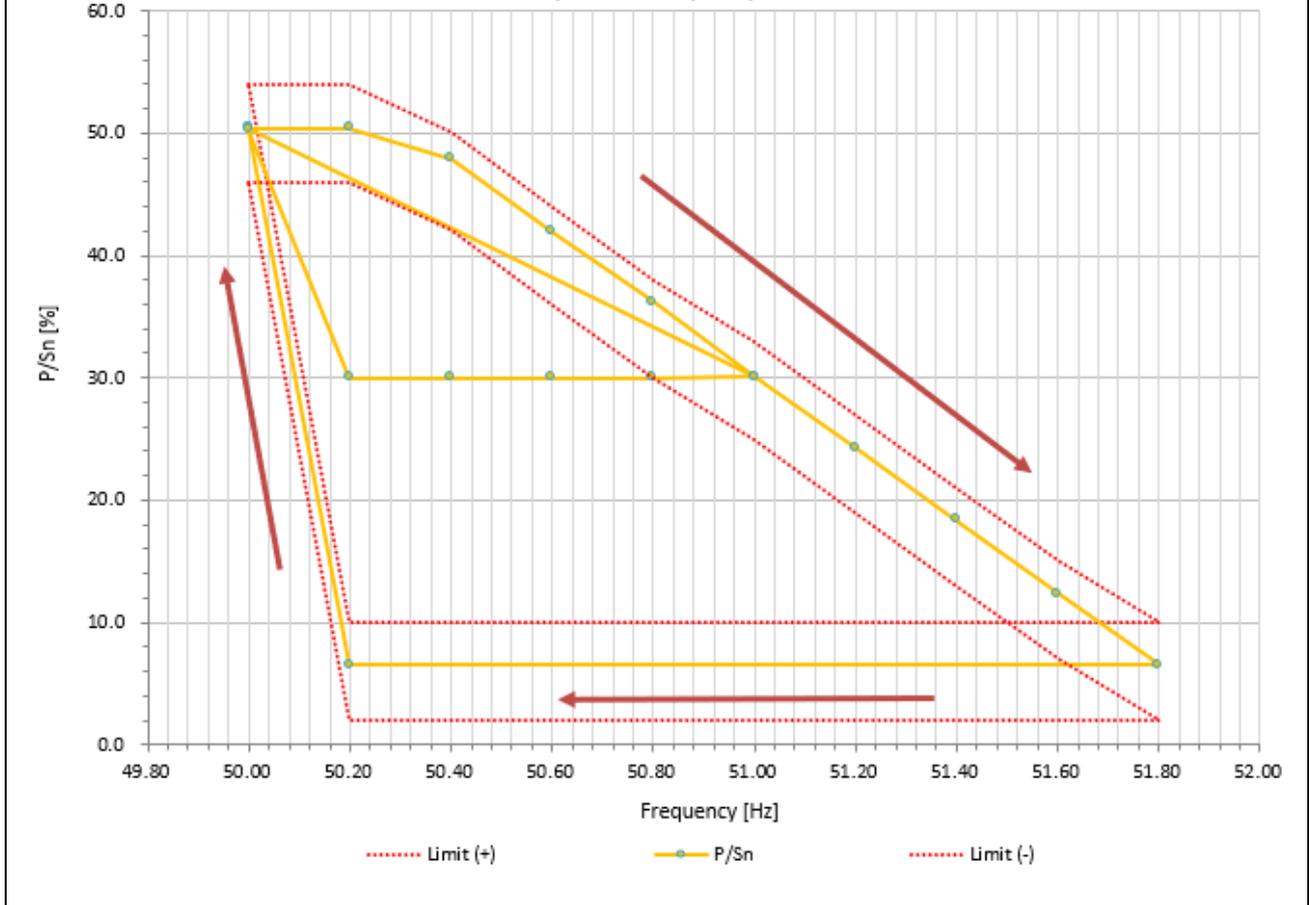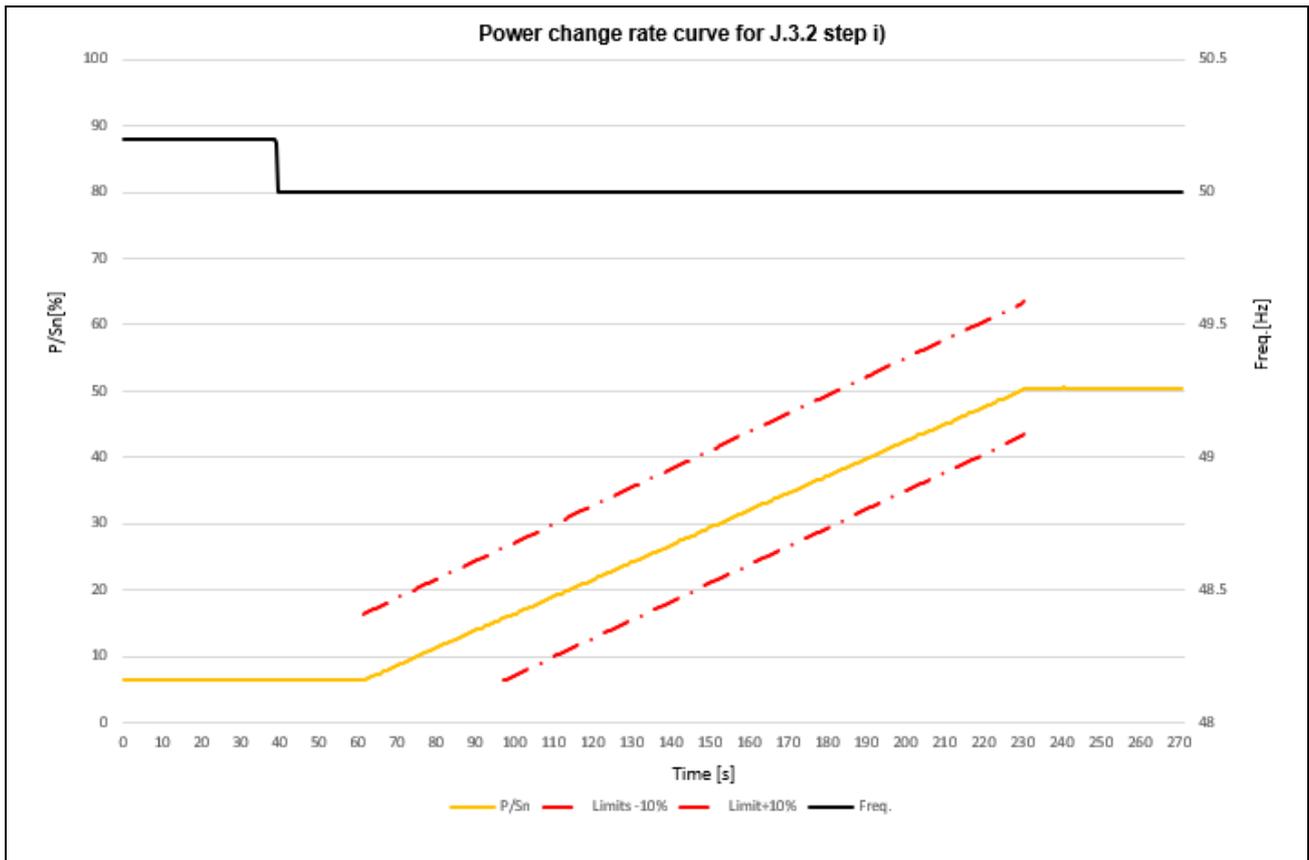
Appendix J.3.4	TABLE: Test for an decrease in frequency for inverters without energy storage			P
LFSM-O curve settings: Australia A	Points	f_{LLCO}	$F_{stop-ch}$	f_{Pmax}
	Hz	49.75	--	48.0
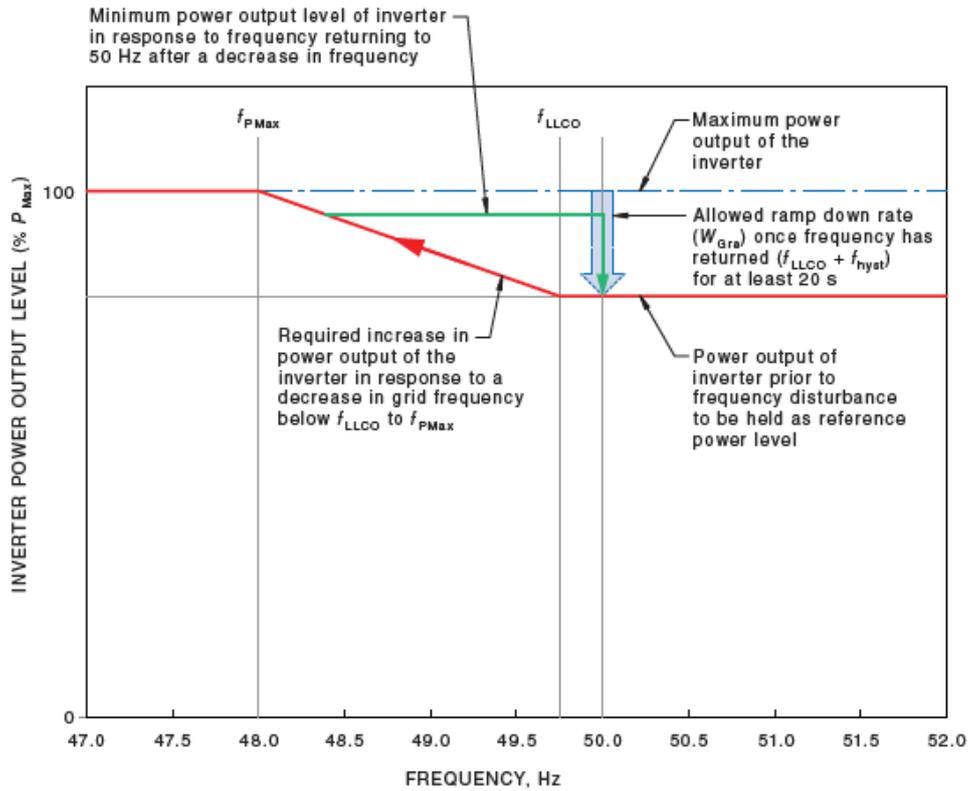
Figure 4.1 — Example frequency response for a decrease in frequency for an inverter that has a reduced output

$$P_{out} = P_{ref} + \left[\left(P_{max} - P_{ref} \right) \left(\frac{ \left(f_{LLCO} - f \right) }{ \left(f_{LLCO} - f_{Pmax} \right) } \right) \right]$$

Test Conditions	Measurements				Target value	Δ	Limit		
f [Hz]	P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/Pn [%]	Δ P/Sn [%]	Δ P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]
50.0	58.74	0	0	--	60	-1.26			
49.8	58.77	0.2	6	--	60	-1.23			
49.6	63.38	0.2	5	--	63	0.38			
49.4	68.78	0.2	4.2	--	68	0.78			
49.2	73.55	0.2	5	--	73	0.55			
49.0	78.09	0.2	5	--	77	1.09			
48.8	83.10	0.2	5	--	82	1.10	≤ ±4	≤ 1	≤ 10
48.6	87.80	0.2	4	--	86	1.80			
48.4	92.67	0.2	5	--	91	1.67			
48.2	96.84	0.2	6	--	95	1.84			
48.0	100.20	0.2	5	--	100	0.20			
47.8	100.20	0	0	--	100	0.20			
48.0	100.16	--	--	--	100	0.16			

48.2	100.17	--	--	--	100	0.17
48.4	100.17	--	--	--	100	0.17
48.6	100.17	--	--	--	100	0.17
48.8	100.17	--	--	--	100	0.17
49.0	100.17	--	--	--	100	0.17
49.2	100.15	--	--	--	100	0.15
49.4	100.16	--	--	--	100	0.16
49.6	100.16	--	--	--	100	0.16
49.8	100.16	--	--	--	100	0.16
50.0	59.01	--	--	15.87	60	-0.99
Ramp to 49.0Hz with 4Hz/s	78.27	0.2	4	--	77	1.27
49.2	78.23	--	--	--	77	1.23
49.4	78.13	--	--	--	77	1.13
49.6	78.10	--	--	--	77	1.10
49.8	78.10	--	--	--	77	1.10
50.0	58.96	--	--	15.28	60	-1.04

Following configuration shall be inspected

Australia A	Available / ~~Not available~~	Australia B	Available / ~~Not available~~
Australia C	Available / ~~Not available~~	New Zealand	Available / ~~Not available~~

LFSM-O Configurable range	Points	f_{LLCO}	$F_{stop-ch}$	f_{Pmax}
	Hz	49.5-49.9	48-49.5	47-49

Diagram

Graph of J.3.4 freq. and power level

Power change rate curve for J.3.4 step j)
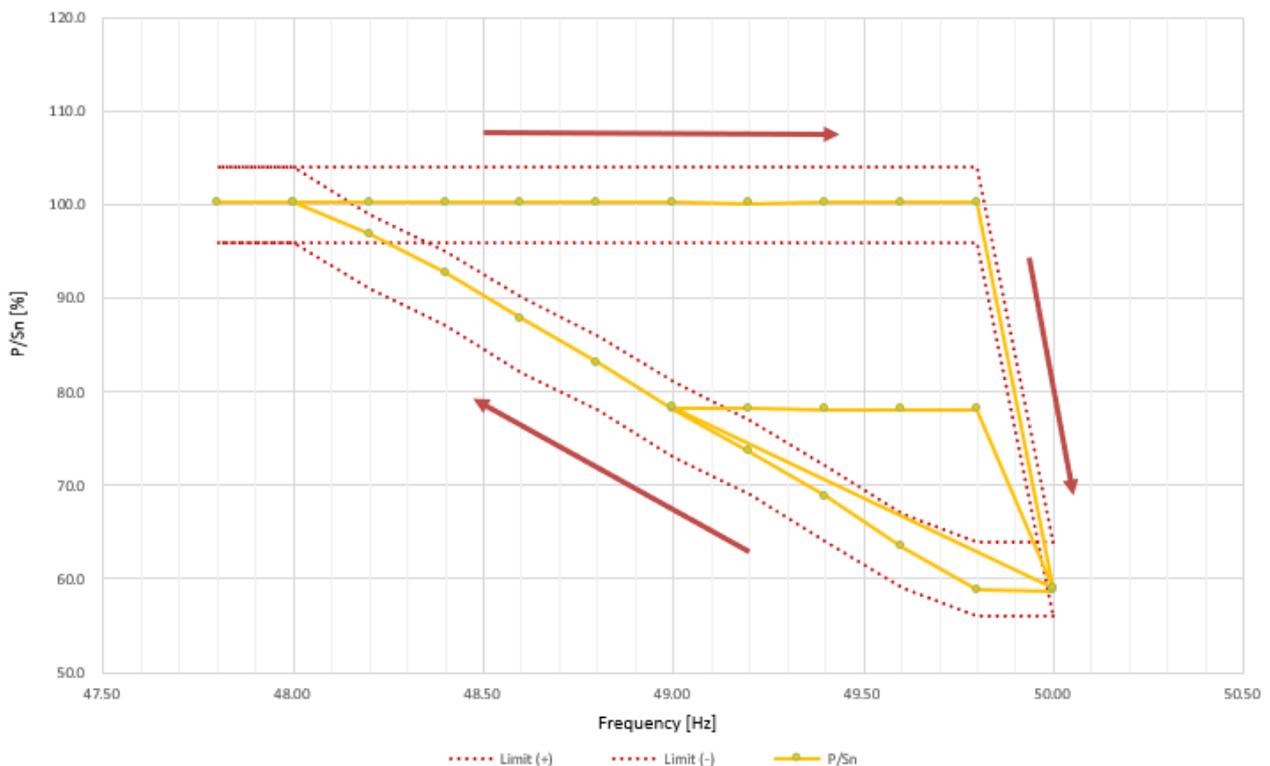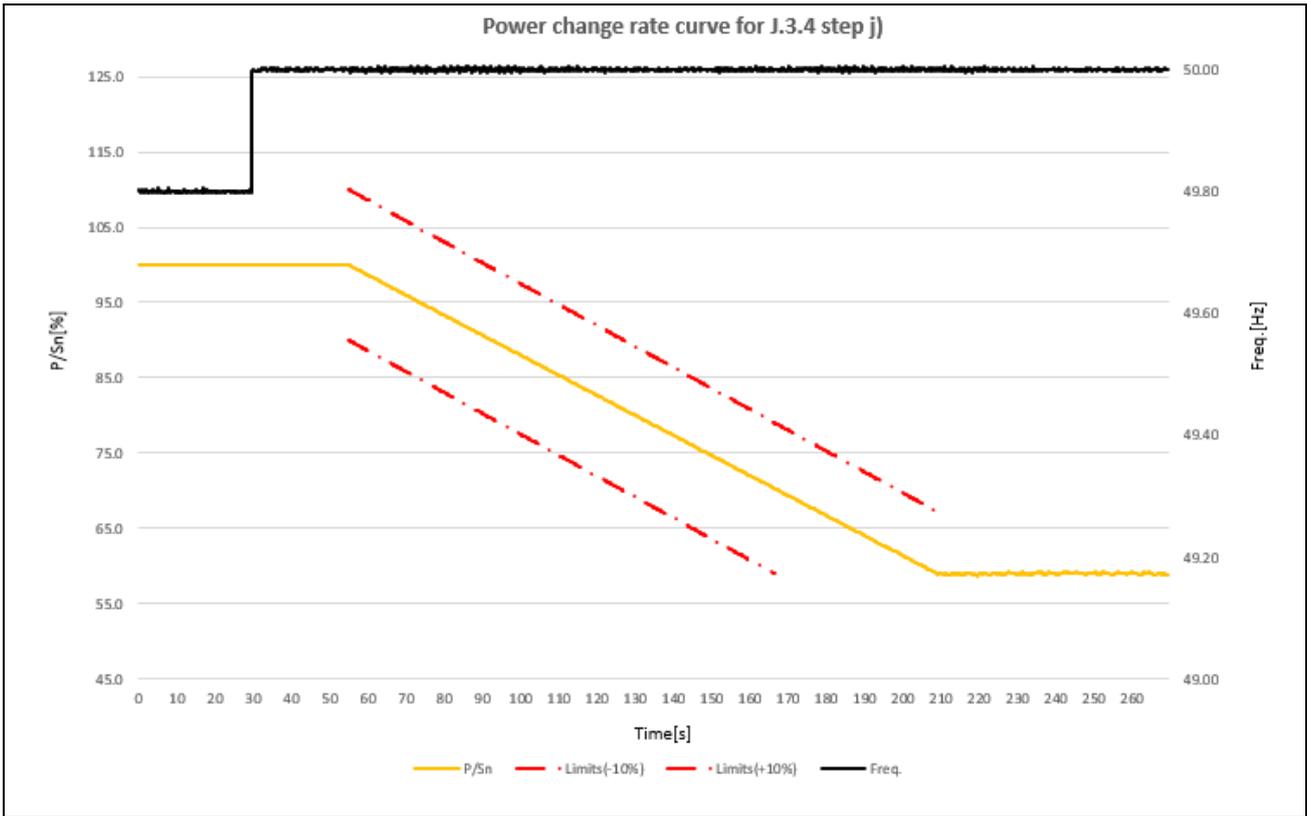
Appendix J.3.6	TABLE: Test for an increase in frequency for inverters with energy storage			P
LFSM-O curve settings: Australia A	Points	f_{ULCO}	$f_{trasition}$	f_{Pmin}
	Hz	50.25	50.75	52.0
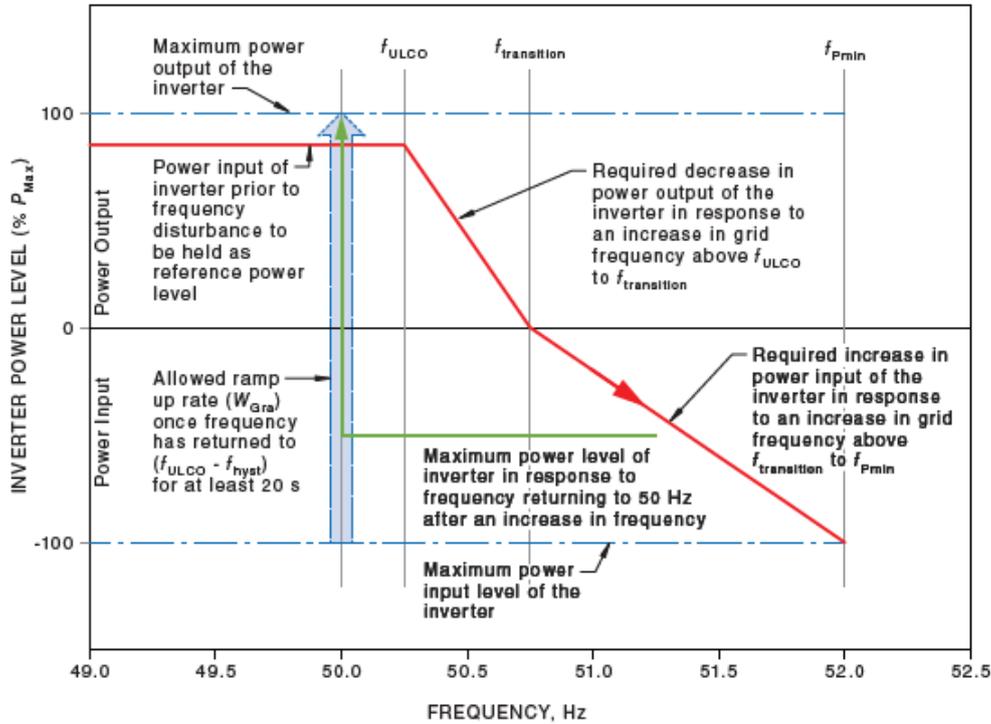
Figure 4.4 — Example frequency response for an increase in frequency for the multiple mode inverter with energy storage for $f_{transition}$ of 50.75 Hz

$$P_{out} = P_{ref}\left[1 - \frac{(f - f_{ULCO})}{(f_{transition} - f_{ULCO})}\right]$$

$$P_{charge} = \begin{cases} P_{rated\text{-}ch}\left[\dfrac{(f - f_{transition})}{(f_{Pmin} - f_{transition})}\right] & \text{if inverter generating before disturbance} \\ P_{ref\text{-}ch} + (P_{rated\text{-}ch} - P_{ref\text{-}ch})\left[\dfrac{(f - f_{transition})}{(f_{Pmin} - f_{transition})}\right] & \text{if inverter charging before disturbance} \end{cases}$$

$(f_{trans} < f < f_{min})$

Test Conditions	Measurements				Target value	Δ	Limit		
f [Hz]	P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/Sn [%]	Δ P/Sn [%]	Δ P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]
50.0	50.3	0.2	0.2	--	50	0.3			
50.2	50.1	0.2	0.4	--	50	0.1			
50.4	33.5	0.2	2.4	--	35	-1.5			
50.6	14.3	0.2	3.4	--	15	-0.7			
f [Hz]	P/$P_{rated\text{-}ch}$ [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/$P_{rated\text{-}ch}$ [%]	Δ P/$P_{rated\text{-}ch}$ [%]	≤ ±4	≤ 1	≤ 10
50.8	-2.9	0.2	3.2	--	-4	1.1			
51.0	-20.5	0.2	2.6	--	-20	-0.5			
51.2	-38.0	0.2	4.0	--	-36	-2.0			
51.4	-53.5	0.2	4.2	--	-52	-1.5			

51.6	-69.1	0.2	4.2	--	-68	-1.1
51.8	-84.8	0.2	4.4	--	-84	-0.8
51.6	-85.4	--	--	--	-84	-1.4
51.4	-85.4	--	--	--	-84	-1.4
51.2	-85.4	--	--	--	-84	-1.4
51.0	-85.4	--	--	--	-84	-1.4
50.8	-85.4	--	--	--	-84	-1.4
50.6	-85.4	--	--	--	-84	-1.4
50.4	-85.4	--	--	--	-84	-1.4
50.2	-85.4	--	--	--	-84	-1.4
f [Hz]	P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/Sn [%]	Δ P/Sn [%]
50.0	50.0	--	--	16.23	50	0.0
f [Hz]	P/$P_{rated-ch}$ [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/$P_{rated-ch}$ [%]	Δ P/$P_{rated-ch}$ [%]
Ramp to 51.0Hz with 4Hz/s	-20.8	0.2	4.4	--	-20	-0.8
50.8	-20.9	--	--	--	-20	-0.9
50.6	-20.8	--	--	--	-20	-0.8
50.4	-20.8	--	--	--	-20	-0.8
50.2	-20.8	--	--	--	-20	-0.8
f [Hz]	P/Sn [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	P/Sn [%]	Δ P/Sn [%]
50.0	50.1	--	--	16.25	50	0.1

Following configuration shall be inspected						
Australia B	Available / Not available			Australia B	Available / Not available	
Australia C	Available / Not available			New Zealand	Available / Not available	
LFSM-O Configurable range	Points		f_{ULCO}		$f_{trasition}$	f_{Pmin}
	Hz		50.1-50.5		50.5-52.0	51.0-53.0
Diagram						

Graph of J.3.6 freq. and power level

Power change rate curve for J.3.6 step j)

Appendix J.3.8	TABLE: Test for an decrease in frequency for inverters with energy storage			P
LFSM-O curve settings: Australia A	Points	f_{LLCO}	$F_{stop-ch}$	f_{Pmax}
	Hz	49.75	49.0	48.0
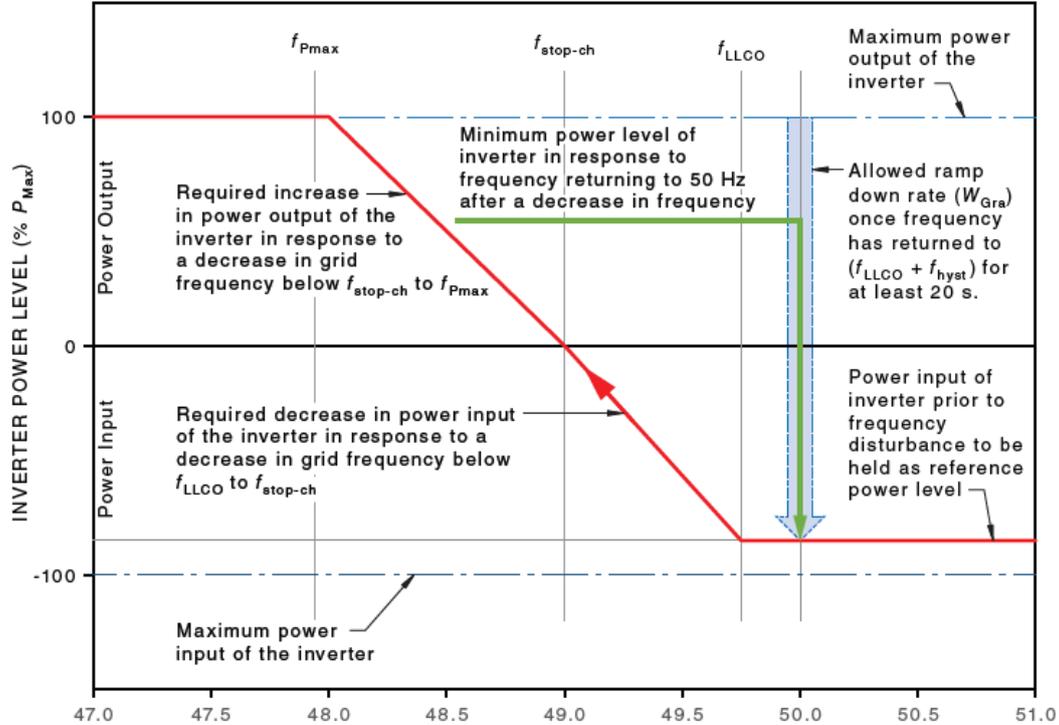
$$P_{charge} = P_{ref-ch}\left[1 - \frac{(f_{LLCO} - f)}{(f_{LLCO} - f_{stop-ch})}\right]$$ ($f_{stop-ch} < f < F_{LLCO}$)

$$P_{out} = \begin{cases} P_{max}\left[\dfrac{(f_{stop-ch} - f)}{(f_{stop-ch} - f_{Pmax})}\right] & \text{if inverter charging before disturbance} \\ P_{ref} + (P_{max} - P_{ref})\left[\dfrac{(f_{stop-ch} - f)}{(f_{stop-ch} - f_{Pmax})}\right] & \text{if inverter generating before disturbance} \end{cases}$$

($f_{max} < f < F_{stop-ch}$)

Test Conditions	Measurements				Target value	Δ	Limit		
f [Hz]	P/P$_{rated-ch}$ [%]	T$_{initial}$ [s]	T$_{stabilize}$ [s]	Power ramp [%/min]	P/P$_{rated-ch}$ [%]	Δ P/P$_{rated-ch}$ [%]	Δ P/Sn [%]	T$_{initial}$ [s]	T$_{stabilize}$ [s]
50.0	-50.4	0.2	0.2	--	-50	-0.4			
49.8	-50.4	0.2	0.2	--	-50	-0.4			
49.6	-41.3	0.2	2.8	--	-40	-1.3			
49.4	-27.4	0.2	1.0	--	-26	-1.4			
49.2	-14.3	0.2	1.4	--	-13	-1.3			
f [Hz]	P/Sn [%]	T$_{initial}$ [s]	T$_{stabilize}$ [s]	Power ramp [%/min]	P/Sn [%]	Δ P/Sn [%]	≤ ±4	≤ 1	≤ 10
49.0	-0.8	0.2	3.0	--	0	-0.8			
48.8	20.1	0.2	2.8	--	20	0.1			
48.6	40.3	0.2	1.0	--	40	0.3			
48.4	61.4	0.2	1.0	--	60	1.4			

48.2	81.6	0.2	1.0	--	80	1.6
48.0	99.7	0.2	1.0	--	100	-0.3
47.8	100.0	0.2	0.2	--	100	0.0
48.0	100.0	--	--	--	100	0.0
48.2	100.0	--	--	--	100	0.0
48.4	100.0	--	--	--	100	0.0
48.6	100.0	--	--	--	100	0.0
48.8	100.0	--	--	--	100	0.0
49.0	100.0	--	--	--	100	0.0
49.2	100.0	--	--	--	100	0.0
49.4	100.0	--	--	--	100	0.0
49.6	100.0	--	--	--	100	0.0
49.8	100.0	--	--	--	100	0.0
f [Hz]	$P/P_{rated\text{-}ch}$ [%]	$T_{initial}$ [s]	$T_{stabilize}$ [s]	Power ramp [%/min]	$P/P_{rated\text{-}ch}$ [%]	$\Delta P/P_{rated\text{-}ch}$ [%]
50.0	-50.4	--	--	16.24	-50	-0.4
Ramp to 49.2Hz with 4Hz/s	-13.9	0.2	1.6	--	-13	-0.9
49.4	-13.9	--	--	--	-13	-0.9
49.6	-13.9	--	--	--	-13	-0.9
49.8	-13.9	--	--	--	-13	-0.4
50.0	-50.4	0.2	0.2	16.22	-50	-0.4

Following configuration shall be inspected					
Australia B	Available / Not available		Australia B		Available / Not available
Australia C	Available / Not available		New Zealand		Available / Not available
LFSM-O Configurable range	Points		f_{LLCO}	$F_{stop\text{-}ch}$	f_{Pmax}
	Hz		49.5-49.9	48-49.5	47-49
Diagram					

Graph of J.3.8 freq. and power level

Power change rate curve for J.3.8 step k)

Appendix L.4.2.1		TABLE: Soft export limit control											P
			Measurements					Limit					
Step	Soft export limit [%]	Test condition	Time [s]	DUT Output power P/Sn	DUT Output power Q/Sn	Grid power P/Sn	Grid power Q/Sn	Time[s]	DUT Output power P/Sn	DUT Output power Q/Sn	Grid power P/Sn	Grid power Q/Sn	
(d)	+25%	P_{EUT}=100%Pn P load=100%Pn Q_L load=0%Pn Q_c load=0%Pn	--	99.9%	1.4%	-0.8%	0.4%	--	100 ± 4%	0 ± 4%	0 ± 5%	--	
(f)	+25%	P_{EUT}=100%Pn P load=100%Pn Q_L load=20%Pn Q_c load=0%Pn	2.4	99.9%	1.4%	-1.2%	20.9%	≤15s	100 ± 4%	0 ± 4%	0 ± 4%	-20 ± 4%	
(h)	+25%	P_{EUT}=100%Pn P load=50%Pn Q_L load=20%Pn Q_c load=0%Pn	2.4	74.9%	0.7%	24.9%	20.9%	≤15s	75 ± 4%	0 ± 4%	25 ± 4%	-20 ± 4%	
(i)	+25%	P_{EUT}=100%Pn P load=0%Pn Q_L load=20%Pn Q_c load=0%Pn	3	24.9%	0.6%	24.8%	21.1%	≤15s	25 ± 4%	0 ± 4%	25 ± 4%	-20 ± 4%	
(l)	+25%	P_{EUT}=100%Pn P load=100%Pn Q_L load=20%Pn Q_c load=0%Pn	6.7	100.0%	1.3%	-0.1%	20.6%	≤15s	100 ± 4%	0 ± 4%	0 ± 4%	-20 ± 4%	
(n)	+25%	External signal interrupt	2.9	25.0%	0.9%	-74.3%	20.0%	≤15s	25 ± 4%	0 ± 4%	-75 ± 4%	-20 ± 4%	
(p)	+25%	External signal recover	16.23%Pn/min					16.67%Pn/min					
(d)	0%	P_{EUT}=100%Pn P load=100%Pn Q_L load=0%Pn Q_c load=0%Pn	--	100.0%	1.3%	0.5%	0.4%	--	100 ± 4%	0 ± 4%	0 ± 4%	--	
(f)	0%	P_{EUT}=100%Pn P load=100%Pn Q_L load=20%Pn Q_c load=0%Pn	0.3	100.0%	1.3%	-0.2%	-20.4%	≤15s	100 ± 4%	0 ± 4%	0 ± 4%	-20 ± 4%	

(h)	0%	P_EUT=100%Pn P load=50%Pn Q_L load=20%Pn Q_c load=0%Pn	2.5	49.0%	0.7%	-0.8%	20.8%	≤15s	50 ± 4%	0 ± 4%	0 ± 4%	-20 ± 4%
(i)	0%	P_EUT=100%Pn P load=0%Pn Q_L load=20%Pn Q_c load=0%Pn	3.2	0.0%	1.4%	0.0%	21.0%	≤15s	0 ± 4%	0 ± 4%	0 ± 4%	-20 ± 4%
(l)	0%	P_EUT=100%Pn P load=100%Pn Q_L load=20%Pn Q_c load=0%Pn	7.1	100.0%	1.3%	-0.1%	20.6%	≤15s	100 ± 4%	0 ± 4%	0 ± 4%	-20 ± 4%

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Appendix L.4.2.2		TABLE: Hard export limit control										P
			Measurements					Limit				
Step	Hard export limit [%]	Test condition	Time [s]	DUT Output power P/Sn	DUT Output power Q/Sn	Grid power P/Sn	Grid power Q/Sn	Time	DUT Output power P/Sn	DUT Output power Q/Sn	Grid power P/Sn	Grid power Q/Sn
(d)	+50%	P_{EUT}=100%Pn P load=100%Pn Q_L load=0%Pn Q_c load=0%Pn	--	100.6%	1.7%	-0.3%	-1.8%	--	100 ± 4%	0 ± 4%	0 ± 5%	--
(f)	+50%	P_{EUT}=100%Pn P load=100%Pn Q_L load=0%Pn Q_c load=20%Pn	--	100.6%	1.7%	-0.2%	-20.8%	--	100 ± 4%	0 ± 4%	0 ± 4%	20 ± 4%
(h)	+50%	P_{EUT}=100%Pn P load=55%Pn Q_L load=0%Pn Q_c load=20%Pn	--	100.5%	1.5%	45.4%	-20.7%	--	100 ± 4%	0 ± 4%	45 ± 4%	20 ± 4%
(j)	+50%	Reducing test load in steps until the ADD operated	2.4	0.0%	0.9%	-48.5%	-21.0%	≤5s	0%	0%	-50 ± 4%	20 ± 4%
(l)	+50%	P_{EUT}=100%Pn P load=100%Pn Q_L load=0%Pn Q_c load=20%Pn (EUT recovered)	61	--	--	--	--	≥60s	--	--	--	--
(m)	+50%	P_{EUT}=100%Pn P load=100%Pn Q_L load=0%Pn Q_c load=20%Pn (Ramp rate after reconnection)	16.18%Pn/min					16.67%Pn/min				
(n)	+50%	External signal interrupt	2.4	-	-	-	-	≤5s	--	--	--	--
(o)	+50%	External signal recovered	61	-	-	-	-	≥60s	--	--	--	--
(p)	5%	Reducing test load in steps until the ADD operated	2.1	0.0%	0.9%	-93.6%	-20.9%	≤5s	0.0%	0.0%	-95 ± 4%	20 ± 4%

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Appendix L.4.2.3			TABLE: Generation limit control														P
			Measurements							Limit							
Step	Hard/soft generation limit	Test condition	Time [s]	DUT Output power P/Sn	DUT Output power Q/Sn	DUT Output power S/Sn	Grid power P/Sn	Grid power Q/Sn	Grid power S/Sn	Time	DUT Output power P/Sn	DUT Output power Q/Sn	DUT Output power S/Sn	Grid power P/Sn	Grid power Q/Sn	Grid power S/Sn	
(d)	+100%	P_EUT=100%Pn P_ac2=25%Pn	--	74.9%	0.8%	74.9%	99.8%	-1.6%	99.8%	--	100 +4/-29%	0 ± 4%	100 +4/-29%	125 +5/-29%	0 ± 4%	125 +5/-29%	
(e)	+100%	P_EUT=100%Pn P_ac2=25%Pn	1.2	74.9%	0.8%	74.9%	99.8%	-1.7%	99.8%	≤15s	75 ± 4%	0 ± 4%	75 ± 4%	100 ± 4%	0 ± 4%	100 ± 4%	
(g)	+100%	P_EUT=100%Pn P_ac2=75%Pn	3.2	24.8%	0.8%	24.8%	99.8%	-1.7%	99.8%	≤15s	25 ± 4%	0 ± 4%	25 ± 4%	100 ± 4%	0 ± 4%	100 ± 4%	
(i)	+100%	P_EUT=100%Pn P_ac2=95%Pn	1.0	4.7%	1.0%	4.8%	99.8%	-1.7%	99.8%	≤15s	5 ± 4%	0 ± 4%	5 ± 4%	100 ± 4%	0 ± 4%	100 ± 4%	
(k)	+100%	P_EUT=100%Pn P_ac2=97.5%Pn	0.2	2.5%	1.3%	2.8%	99.7%	-1.9%	99.7%	≤15s	2.5 ± 4%	0 ± 4%	0%<P<6.5%	100 ± 4%	0 ± 4%	100 ± 4%	
(k)	+100%	P_EUT=100%Pn P_ac2=100%Pn	0.2	0.9%	1.3%	1.6%	99.5%	-2.0%	99.6%	≤15s	0 ± 4%	0 ± 4%	0%<P<4%	100 ± 4%	0 ± 4%	100 ± 4%	
(k), (i)	+100%	P_EUT=100%Pn P_ac2=102.5%Pn (ADD operated)	16.6	0.0%	1.3%	1.3%	102.2%	-1.9%	102.3%	15s < t < 20s	0.0%	0.0%	0.0%	100 ± 4%	0 ± 4%	100 ± 4%	
(n)	+100%	P_EUT=100%Pn P_ac2=25%Pn (EUT recovered)	61	--	--	--	--	--	--	≥60s	--	--	--	--	--	--	
(o)	+100%	Ramp rate after reconnection	16.23%Pn/min.							16.67%Pn/min							
(p)	+100%	External signal interrupt	2.2	--	--	--	--	--	--	≤5s	--	--	--	--	--	--	
(q)	+100%	External signal recover	61	--	--	--	--	--	--	≥60s	--	--	--	--	--	--	